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*Cypress' MRAM disclosures detail its flaws.*

Cypress Semiconductor Corporation (NYSE: CY, \$9.60) made a presentation at three conferences between August 12 and September 8, 2004 containing a technical description of Cypress' Magnetoresistive Random Access Memory ("MRAM") chip. Those disclosures constitute Cypress' most revealing disclosures concerning its MRAM effort. We have conducted a full, technical review of Cypress' new MRAM disclosures.

Cypress' own presentation shows that its hoped-for MRAM has a larger die size, less capacity, is slower, more expensive to manufacture, less dense and requires a higher operating voltage than even current SRAM chips. Cypress' unavailable MRAM product is inferior and not comparable to MRAM from Freescale Semiconductor, Inc. (NYSE: FSL, \$14.95) and International Business Machines Corporation (NYSE: IBM, \$86.37) and Infineon Technologies AG (NYSE: IFX, \$10.07).

The chart titled "Life Cycle of an SRAM" in Cypress' 1999 Annual Report shows that in 1988 Cypress produced 712 256Kbit SRAM die per wafer at a cost of \$1.50 per chip. In 2000 Cypress produced 6,374 256Kbit SRAM die per wafer, or 8.9 times more die per wafer, at a cost of \$0.15 per chip. In contrast, Cypress' unavailable MRAM chip yields at best approximately 1,200 die per wafer, or 80% less than Cypress' own four year old SRAM chip. Furthermore Cypress' unavailable MRAM chip has a larger cell size, needs more error correction circuitry ("ECC"), uses a large outdated manufacturing process, requires higher voltage and has more transistors per cell, in addition to having over 80% lower yield.

Below is a description of the disclosures contained in Cypress' presentations with links to the source materials.

**LARGE MEMORY CELL SIZE**

The "cell size" shown on <http://www.asensio.com/Report-images/CY/CYS64.pdf> of Cypress' presentation discloses that its 256Kbit MRAM cell has grown larger in each of its three generations from 11.5 $\mu$ <sup>2</sup>; to 24 $\mu$ <sup>2</sup>;. This cell size is an average of 16.9 times larger than other MRAM chips. This means that Cypress fits fewer die on each wafer increasing the manufacturing costs per die with each new MRAM generation and decreasing capacity. By contrast the cell size of Freescale's 4Mbit MRAM product is 1.55 $\mu$ <sup>2</sup>;. IBM and Infineon have demonstrated their 16Mbit MRAM product with a reported cell size of 1.42 $\mu$ <sup>2</sup>;

**NEED FOR ERROR CORRECTION**

One reason that Cypress' MRAM cell is larger than a normal chip is that it has not been able to solve its "soft error" problem. "Repairability" on <http://www.asensio.com/Report-images/CY/CYS64.pdf> of the presentation has grown from 2 rows to 4 rows to 64 subrows. Cypress' MRAM needs redundant ECC to compensate for its MRAM's unreliable performance. The ECC uses precious space and makes Cypress' MRAM cells larger and increases its manufacturing costs.

**LARGE MANUFACTURING PROCESS**

Cypress' MRAM is built using a 0.42 $\mu$  manufacturing process. SRAM is commonly built using a 0.25 $\mu$  process. Freescale's and IBM and Infineon's MRAM products are built using a 0.18 $\mu$  process.

**HIGH VOLTAGE REQUIREMENT**

MRAM has been referred to as the "Holy Grail" of memory because ultimately it would replace DRAM, Flash and SRAM. However Cypress' MRAM operates at 5 volts ("V") while the trend in memories today is towards 3V operation. Our survey of memory chips by leading manufacturers Intel Corporation (NASDAQ: INTC, \$20.42), Samsung Electronics Co. Ltd., Renesas Technology and Micron Technology, Inc. (NYSE: MU, \$12.10) found that the vast majority of DRAM, Flash and SRAM operate at 3.6V or less.

**LARGE NUMBER OF TRANSISTORS**

NVE Corporation's (NASDAQ: NVEC, \$36.71) patents describe a one transistor per memory cell architecture. "Architecture" on <http://www.asensio.com/Report-images/CY/CYS64.pdf> of the presentation shows that its current 256kBit MRAM cell is "3T2R." According to Cypress "3T2R stands for memory cell with three transistors and two resistors." This implies that Cypress is not even using NVE's self-proclaimed MRAM IP, which is actually 36 years old and in the public domain.

**LOW QUALITY YIELD**

<http://www.asensio.com/Report-images/CY/CYS63.pdf> of the presentation is titled "MRAM Yield" and contains a yield map of Cypress' actual six inch MRAM wafer. Cypress' MRAM wafers fit approximately 1,750 die per wafer. Only 40 die of Cypress' MRAM yield are "virgin" while 1,173 die of the yield are "repairable."

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