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NVEC's MRAM patents are immaterial and unenforceable.

NVE Corporation's (NASDAQ: NVEC, $37.99) market value is entirely based on vague claims that it possesses patents that are valuable to Magnetoresistive Random Access Memory's ("MRAM") developers. This report analyzes the enforceability, significance and materiality of the patents that NVE holds that it claims are pertinent to MRAM. The patents constitute the basis for its crafty and unsubstantiated MRAM intellectual prpoerty ("IP") claims.

The granting of a patent does not in any way assure enforceability of the claims or commercial value. Between 1983 and 2003 the U.S. Patent and Trademark Office issued an average of 138,550 patents annually. This report examines the claimed functionality of two NVE patents that it has alleged to be applicable to the design or production of an MRAM chip and their enforceability.

Any discussion about the value of NVE's alleged MRAM IP is overshadowed by the simple fact that NVE's claims were first patented by International Business Machines Corporation (NYSE: IBM, $86.72) in 1968, are in the public domain and are in use worldwide for free. We fail to see any basis for MRAM's true developers to pay NVE for a 36-year-old invention that is in the public domain and that has no bearing on MRAM's core enabling inventions.

DESCRIPTION OF PATENTS

On November 8, 1999 NVE filed the application for US Patent 6,275,411 ("Patent 411"). On August 15, 2001 NVE announced the issuance of Patent 411, titled "Spin dependent tunneling memory." NVE stated that Patent 411 covers features used in "many publicly-disclosed development programs by a number of organizations developing magnetoresistive tunnel junction (MTJ) MRAMs." This patent describes a memory cell with an MTJ and transistor circuit.

On June 26, 2001 NVE filed its application for a continuation of Patent 411. On February 28, 2002 NVE announced the issuance of US Patent 6,349,053 ("Patent 053"), titled "Spin Dependent Tunneling Memory." NVE calls Patent 053 a "watershed MRAM patent." In the release NVE claimed that Patent 053 "covers transistor-selected magnetic memory cells, a concept being used by a number of organizations developing MRAM." Patents 411 and 053 form the basis for NVE's claim that it possesses valuable MRAM IP.

It is important to note that Patent 411 and Patent 053 have absolutely nothing to do with any of the 13 major inventions that are commonly credited with permitting the creation of magnetic (or spin) memory cells. Click here to read History of MTJ MRAM Developments. It is also important to note that none of NVE's patents cover any chip design, or any magnetic (or spin) memory cell design or even any design to write to, store and read data from a magnetic (or spin) memory cell. Below we detail the contents of NVE's patents to show their commonness and their immaterial nature.

Click here to read NVE's Patent

411, August 15th press release, Patent 053, and February 28th press release.

NVE PATENTS DO NOT COVER MRAM MEMORY CELLS

The one transistor per bit read addressing-scheme described in Patent 411 and Patent 053 has been used in Dynamic RAM ("DRAM") since the 1960s. Dr. Robert Dennard, an IBM Fellow, invented the one transistor DRAM in 1966. In the NVE patents, the memory cell in a DRAM chip is simply and immaterially replaced by a magnetic memory (or spin) cell. Patent 411 and Patent 053 are a simple application of the preexisting DRAM addressing-scheme to an existing non-NVE related MRAM memory cell.

NVE's patents do not cover any inventions used to create a magnetic (or spin) memory cell. Using magnetism (or spin) as the memory cell is what makes MRAM chips possible. NVE has no patents on a magnetic (or spin) memory cell.

PRIOR ART

The mere fact that the patent was issued does not in any way assure that a patent is enforceable or exclude challenges based on prior art that NVE did not cite. In fact, any party (not just a patent holder or the owner of the prior art) may submit prior art to the U.S. Patent and Trademark Office ("Office") for inclusion in an existing patent's claims. The Office's Manual of Patent Examining Procedure ("MPEP") specifically states that "Any person at any time may cite to the Office in writing prior art consisting of patents or printed publications which that person believes to have a bearing on the patentability of any claim of a particular patent." Click here to read MPEP Chapter 2200.

NVE's MRAM patents are both preceded by the following patent filing and publications. These publications and patent therefore constitute prior art.

A Motorola, Inc. (NYSE: MOT, $16.87) US Patent 6,055,178 ("Patent 178"), which uses a Motorola designed MRAM memory cell and a transistor as a reference memory element, was filed on December 18, 1998 almost 11 months prior to the date of the NVE application and issued on April 25, 2000. The circuit drawn in the Motorola patent clearly anticipates the circuits that NVE describes in its patents. Click here to read Motorola's Patent 178. After the filing Motorola published papers. Even those papers pre-date NVE's patent.

A Motorola paper, titled "Progress and Outlook for MRAM Technology," published in the September 1999 IEEE Transactions on Magnetics ("1999 Motorola Paper"). This paper shows a transistor-selected bit-addressable Motorola-designed MRAM cell. The circuits described in NVE's patents and the circuits described in Motorola's paper, which pre-dates NVE's patent application date by two months, are identical. Click here to read the 1999 Motorola Paper.

An IBM paper titled, "Magneto-Resistive IC Memory Limitations and Architecture Implication,"

presented in August 1998, published in the 1998 International NonVolatile Memory Technology Conference Technical Digest ("1998 IBM Paper") presents an overview of an IBM designed MRAM cell and describes the use of a transistor as a switch. This paper precedes the date of the NVE application file date by nearly 15 months. Click here to read the 1998 IBM Paper.

The two published papers and patent above predate and were publicly available before the filing of NVE's first MRAM patent application. The above prior art provides documentation that NVE's claims were conceived and published by someone else first. The mere fact that a patent was issued does not preclude a challenge to NVE's patents based on these publications. Furthermore, the prior art questions the likelihood that NVE invented the claims in Patent 411 and Patent 053. It is even more questionable that NVE could successfully litigate a claim based on infringement of Patents 411 and Patent 053 regardless of their value or materiality.

A search of NVE's applications for its alleged MRAM patents did not find citations of the 1999 Motorola Paper, Motorola's Patent 178 or the 1998 IBM Paper as prior art. NVE has an obligation to cite patents and printed publications that are pertinent and applicable to the patent and that may have a bearing on the patentability of any claim in the patent. NVE could have included the prior art citations and explained how its claims differ from the prior art. It did not.

NVE PATENTS ARE INSIGNIFICANT

The first use of one-transistor to both write and read a single bit dates back to 1966. The invention was patented by IBM in 1968. The invention is now off-patent and in free use in computers worldwide. According to IBM, the single-transistor memory chip set "the stage for development of increasingly dense and cost-effective memory that continues even today at the heart of every succeeding generation of computers." Prior to 1966, six or more transistors were required for the storage of a single bit. The IBM inventor, Dr. Robert Dennard, has been an IBM employee since 1958. Dr. Dennard is today actually working on getting "close to the physical limits" of making chips smaller. We find this poetic given NVE's false claims of being involved in nanotechnology.

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 LIST OF LINKS:

NVE Patent 411:

http://www.asensio.com/Report-images/MRAM/NVEPatent411.pdf

August 15, 2001 NVE press release announcing the issuance of Patent 411:

http://www.asensio.com/Report-images/MRAM/NVETunnelJunction.pdf

NVE Patent 053:

http://www.asensio.com/Report-images/MRAM/NVEPatent053.pdf

February 28, 2002 NVE press release announcing the issuance of Patent 053:
http://www.asensio.com/Report-images/MRAM/NVEWatershed.pdf

History of MTJ MRAM developments:
http://www.asensio.com/Report-images/MRAM/MRAMTimeline.pdf

Manual of Patent Examining Procedure:
http://www.uspto.gov/web/offices/pac/mpep/mpep_e8r2_2200_508.pdf

 Motorola US Patent 6,055,178:
http://www.asensio.com/Report-images/MRAM/MOTPatent178.pdf

"Progress and Outlook for MRAM Technology" by Motorola:
http://www.asensio.com/Report-images/MRAM/MOTMRAMpaper.pdf

"Magneto-Resistive IC Memory Limitations and Architecture Implication"
by IBM:
http://www.asensio.com/Report-images/MRAM/IBMMRAMpaper.pdf
