Complex Digital Receiver Processors

Item	ADC[1]	Number of Bits	ADC Sampling Rate		Input Signal Frequency		Nyquist Zones[2]	Max Input Voltage	NSD (1st Nyquist Zone)[3]	Interface
			Min (MSPS)	Max (MSPS)	Min (MHz)	Max (MHz)		Vpp	dBFS/Hz	
ASM-00117-00 Dual Channel DC Coupled 160 MHz Digital Receiver	AD9269	16	10	80	DC	160	1 thu 4	2.0	-153.2	Parallel
ASM-00116-00 Dual Channel 250 MHz Digital Receiver	ADS42LB69	16	10	250	1	250	1 thru 2	2.5	-156.5	LVDS DDR
ASM-00116-10 Dual Channel 400 MHz Digital Receiver						400	1 thru 3	2.0	-154.7	
ASM-00121-00 Quad Channel DC-Coupled 1 GHz Digital Receiver	AD9684	14	250	500	DC	1000	1 thru 4	2.06	-153	LVDS DDR
ASM-00121-10 Quad Channel 2GHz Digital Receiver					1	2000	1 thru 8			
ASM-00124-00 Dual Channel 1.2 GHz Digital Receiver	ADS5409	12	100	900	1	1200	1 thru 3	1.0	-147.5	LVDS DDR
ASM-00135-00 Dual Channel 2 GHz Digital Receiver	AD9680-1250	14	300	1200	10	2000	1 thru 4	1.58	-151.5	JESD204
ASM-00141-00 Dual Channel 2.4 GHz Digital Receiver	AD9689	14	1900	2400	1	9000	1 thru 6	2.0	-154	JESD204
ASM-00125-00 Dual Channel 7.5 GHz Digital Receiver	AD9208	14	2500	3100	10	7500	1 thru 5	2.04	-153.7	JESD204
ASM-00126-00 Single/Dual Channel 2.8 GHz Digital Receiver	ADC12D1800	12	800	3600	10	2800	1, 2	0.8	-150.2	LVDS Parallel
ASM-00127-00 Single/Dual Channel 8 GHz Digital Receiver	ADC12DJ3200	12	800	6400	10	8000	1 thru 3	1.04	-151.4	JESD204

[1] Clock circuitry includes a clock divider circuit allowing for higher input clock.
[2] Nyquist zone for maximum sampling rate
[3] In higher Nyquist zones, internal ADC aperture jitter may increase noise level. See ADC specifications.

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