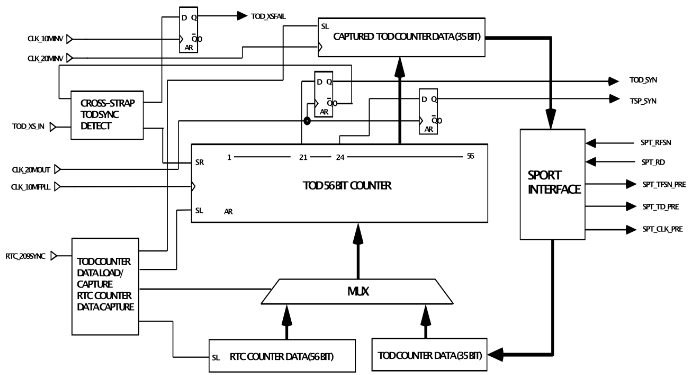

Figure 5.5 – TOD/TSP Sync Generator Logic

5.3.5 Functional Implementation

During initial power up, the Real Time Clock (RTC) counter data is latched into 56 bit registers after reset. The 56 bit registers data is selected by the mux and loaded into the TOD counter. Once the RTC counter data is loaded into the TOD counter, the mux is switched to select the TOD counter data from the SPORT interface. At the same time the TOD counter starts counting. TOD sync is generated using the 21st bit of the 56 bit counter. TSP sync is generated using the 24th bit of the 56 bit counter. Both TOD and TSP syncs are re-clocked at the output by CLK_20MOUT to minimize propagation delay. Using 10MHz clock (100nsec period) and multiplying it by 2 to the 21st power, the TOD sync will have a period of 209.7152msec. The TSP sync will have a period of 1.6772 second. The 56 bit counter is a binary counter; therefore, the pulse width of both TOD and TSP syncs will be at 50% of the period. Software has the ability to read and

5.4.1 Block Diagram

Figure 5.7 shows the RTC counter logic. The RTC 56 bit counter is divided into four ripple counters. Ripple counters are used to reduce the number of registers being clocked by the 10MHz clock and helps to reduce the power dissipation during battery mode.

5.4.2 Functional Implementation

During initial power up (first battery power application) the RTC counter is reset to all zero. Software can write the correct counter data into the RTC counter via SPORT interface. The new RTC counter data are loaded into the RTC counter on the falling edge of the TOD sync. Since the lower 21 bits are all zero during TOD sync, only the upper 35 bits data are sent through the SPORT interface. The new 35 bit data are loaded into the upper 35 bit of the RTC counter, while the lower 21 bit are loaded with zero.

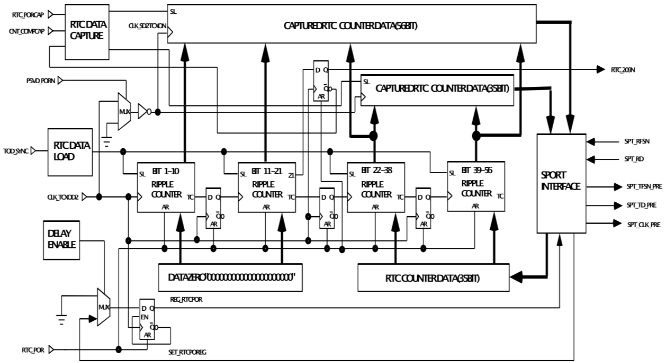

Figure 5.7 – RTC Counter Logic