SPECTRUM DIGITAL INCORPORATED

TMS320C6413/C6418 EVM

Technical Reference

2004 *DSP Development Systems*

TMS320C6413/C6418 EVM
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320C6413/C6418 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320C6413/C6418 Digital Signal Processor.

The TMS320C6413/C6418 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C6413/C6418 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C6413/C6418 will sometimes be referred to as the C641x.

The TMS320C6413/C6418 EVM will sometimes be referred to as the EVM.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C64XX DSP CPU Reference Guide
Texas Instruments TMS320C64XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release

Table 2: Manual History

Revision	History
A	Alpha Release
B	Text Updates

Chapter 1

Introduction to the TMS320C6413/C6418 EVM

Chapter One provides a description of the TMS320C6413/C6418 EVM along with the key features and a block diagram of the circuit board.

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1.0 Key Features

The C6413/C6418 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI C64XX DSP family. The EVM also serves as a hardware reference design for the TMS320C6413/C6418 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

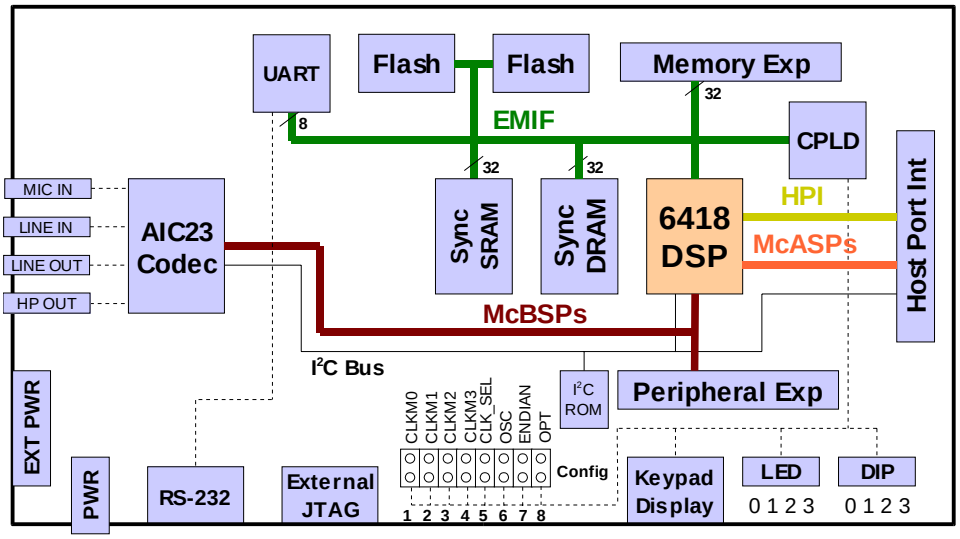


Figure 1-1, Block Diagram C6413/C6418 EVM

The EVM comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas InstrumentsC6413/C6418 DSP operating at 500/600 MHz
- An TLC320AIC23B stereo codec
- 8 Mbytes of synchronous DRAM
- 1 Mbyte of synchronous Burst RAM
- 1 Mbyte of non-volatile Flash memory
- TL16C550 UART with RS-232 Drivers
- 4 user accessible LEDs and DIP switches
- Software board configuration through registers implemented in CPLD
- 128 LCD display and keypad
- Standard expansion connectors for daughter card use

- JTAG emulation via external emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320C6413/C6418 EVM

The DSP interfaces to external SDRAM, SBRAM, Flash memory and an expansion memory interface connector through its 32-bit External Memory Interface (EMIF). The SDRAM accesses are in 32-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 8,16, or 32-bit asynchronous mode in the bottom half of chip enable 1 space. The default mode of the EVM for CE1 is 8 bit mode. The SBRAM is accessed via chip enable 3, if it is not routed to the expansion connector which is controlled by the CPLD control register. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23 codec allows the DSP to transmit and receive analog signals. The I^2C bus is used for the codec control interface and McBSP1 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec input is software selectable between the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors. McBSP1 can be re-routed to the expansion connectors in software.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The EVM includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers.

A separate Keypad/LCD display card is interfaced via CPLD registers and I^2C accesses. This module provides a flexible input/output mechanism for application programs

An included 5V external power supply is used to power the board. On-board voltage regulators provide the +1.2V or +1.4V DSP core voltage, +3.3V digital and +3.3V analog voltages. Voltage supervisors integrated into the regulators monitor voltage regulation, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

1.3 Display/Keypad Overview

The universal display/keypad module interfaces to the EVM via a 16 pin 2mm. ribbon cable.

The display module features a 128 x 64 LCD, 4 I^2C A/D converters, 2 potentiometers, 9 user keys, and a jog wheel. All switches are accessed via the I^2C A/Ds, while the display is accessed via an SPI interface generated internally in the CPLD

Figure 1-2 below shows a block diagram of the display/keypad module.

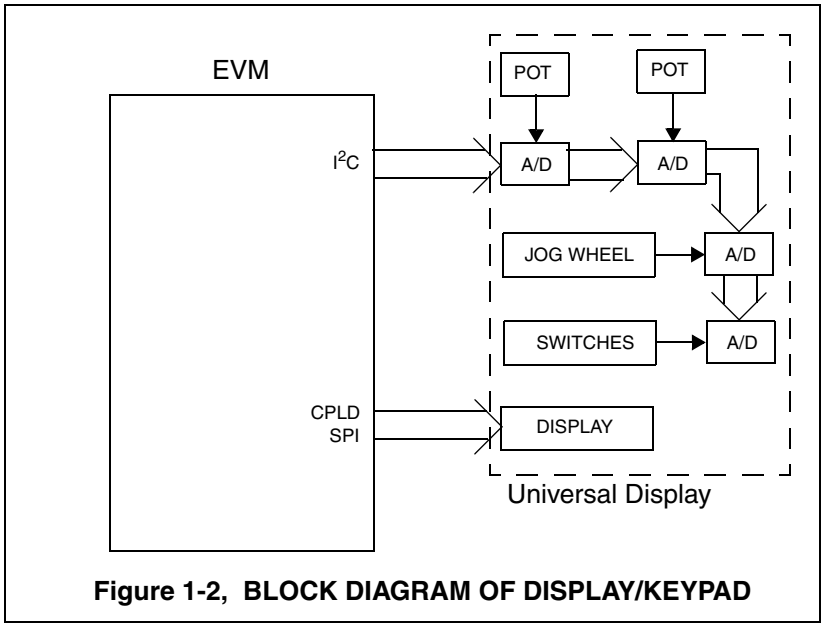


Figure 1-2, BLOCK DIAGRAM OF DISPLAY/KEYPAD

1.4 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development environment and is available in an optional package with the board. Code Composer communicates with the board through the JTAG emulator. To start, follow the instructions in the emulator's Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

1.5 Memory Map

The C64xx family of DSPs has a unified program and data space. Both programs and data can reside anywhere in the unified memory space.

The address reach of the C6413/C6418 is 32 bits. The external memory interface controller (EMIF) divides the off chip address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 20 address bits are driven on the EMIF as address lines while the upper addresses are decoded and driven as the chip enable for that particular region.

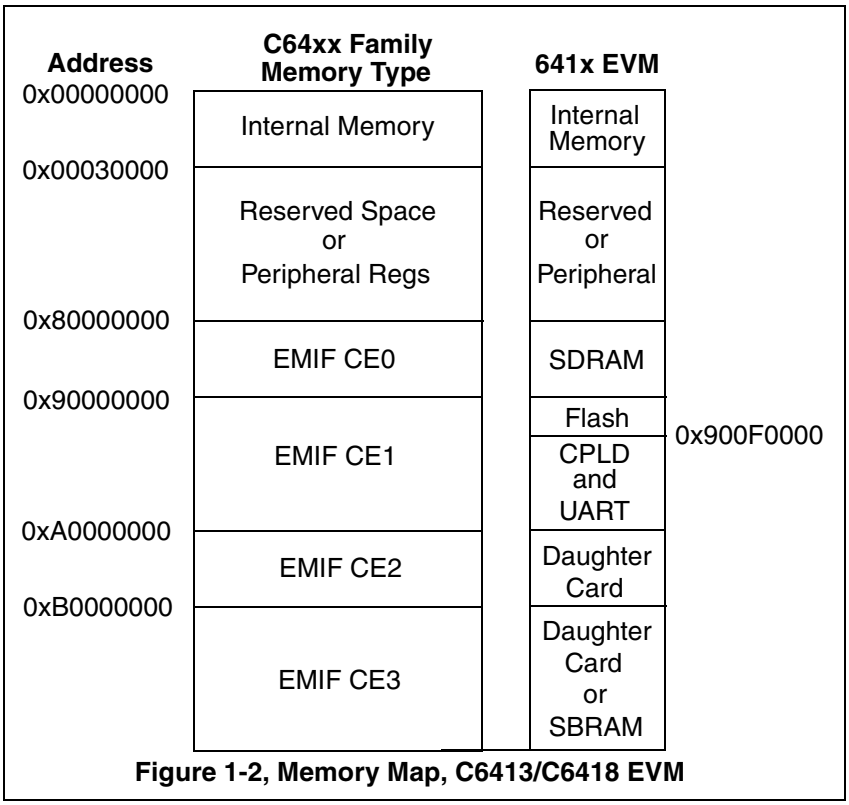


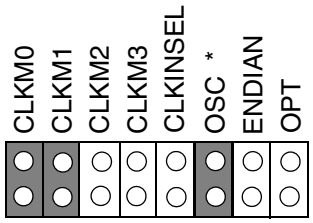
Figure 1-2, Memory Map, C6413/C6418 EVM

The figure above shows a generic memory space map for a C64xx family processor and a second map specific to the components on a C6413/C6418 EVM. The SDRAM occupies chip enable 0. The Flash, UART, and memory mapped registers of the CPLD share CE1. The Flash accesses start at the lower addresses of the CE1, and occupy locations 0x900000000 to 0x900EFFFF and the CPLD in the bottom half. The last remaining locations 0x900F0000 - 0x900FFFFF are mapped to the CPLD and UART. CE2 is used for expansion daughter card access and CE3 is optionally mapped into SBRAM or expansion connector access.

Internal memory on the C6413/C6418 starts at address 0 and takes precedence over any external memory.

1.6 Jumper Settings

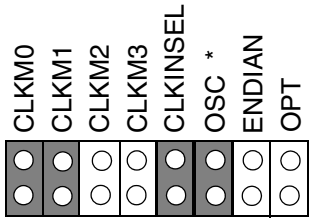
TheC6413/C6418 EVM has 7 on-board CPU configuration jumpers that define the DSP's boot configuration and reset state along with one OPT jumper for user implementation. The figure below shows these jumpers for the C6413.



* Always populated

Figure 1-3, JP4, C6413 DSP Boot Configuration - Default Setting

The figure below shows the jumpers for the C6418.



* Always populated

Figure 1-4, JP4, C6418 DSP Boot Configuration - Default Setting

The jumpers drive signals that directly correspond to the input on one of the DSP's configuration pins. If the jumper is on, the signal is driven to a logic 0. If the jumper is off, the signal is driven to a logic 1.

1.6.1 CLKMODE Multiplier

TheC6413/C6418 has a number of clock multiplier modes that are selected at reset by sampling the CLKMODE[3-0] pins. These pins can be configured with the on-board jumpers. The jumper configuration is shown in the table below.

Table 1: TMS320C6413/C6418 EVM CLKMODE Multiplier

CLKM3	CLKM2	CLKM1	CLKM0	Multiplier
Off	Off	Off	Off	x24 **
Off	Off	Off	On	x22
Off	Off	On	Off	x21
Off	Off	On	On	x20 *
Off	On	Off	Off	x19
Off	On	Off	On	x18
Off	On	On	Off	x16
Off	On	On	On	x12
On	Off	Off	Off	x11
On	Off	Off	On	x10
On	Off	On	Off	x9
On	Off	On	On	x8
On	On	Off	Off	x7
On	On	Off	On	x6
On	On	On	Off	x5
On	On	On	On	Bypass

Note: * default on C6413
** default on C6418

1.6.2 CLKINSEL

The C6413/C6418 has the option of using an external clock oscillator or internal oscillator to operate the PLL which controls the internal CPU clock. This clock is input is selected at reset by the CLKINSEL pin. The EVM provides a configuration jumper to select either the internal or external oscillator which controls the PLL. When CLKINSEL is high (installed) AECLKIN is selected for PLL logic. When CLKINSEL is low (removed) the internal oscillator controls the PLL clock. On theC6413/C6418 EVM AECLKIN is driven by an external 25 Mhz oscillator, the internal oscillator is connected to the external crystal which is 25 Mhz

1.6.3 Oscillator Disable

The OSC_DIS pin is used to enable the on chip oscillator. On the EVM an external oscillator is used as the default configuration. However, the board is populated with a 25 Mhz crystal which is enabled by populating JP4 (11 to 12).

NOTE:
OSC_DIS jumper should always be populated. Disabling the oscillator is for chip test functions only.

For proper operation the CLKINSEL jumper needs to be in configured appropriately to enable the on board oscillator to control the PLL logic when using enabling or disabling the on chip oscillator.

1.6.4 Endian Select

The C6413/C6418 can be operated in little endian or big endian memory modes. The default mode on the EVM is little endian (jumper JP4-13 to 14 removed). When the jumper is installed the board operates in big endian mode.

1.7 EMIFA Configuration Options

External addresses lines A19-A22 are used to configure the boot mode and EMIF clock selection at reset. Four pull up and four pull down resistor locations are available on the EVM to control this configuration. The selections are outlined.

1.7.1 Boot Options

At reset address lines A21 and A22 are sampled to determine the boot option of the processor. although there are four modes available only 2 modes are not reserved. These are 8 bit boot from CE1 which is the default on the EVM and no boot.

1.7.2 EMIFA Clock Select

Address lines A19 and A20 are sampled at reset and determine the EMIF clock configuration selection. The EMIF clock is either a divider of the internal CPU clock controlled by the PLL or is driven directly at the frequency supplied on the AECLKIN pin.

On the EVM an external PLL is available to drive the AECLKIN pin. The default frequency of the ICS512 PLL device is 125 Mhz.

Pull ups and pull downs are provided on the EVM to configure the clock selection. The choices for the EMIF clock configuration are CPUCLK divided by four, CPUCLK divided by six, AECLKIN. The table below details the choices.

Table 2: EMIFA Clock Select

A20	A19	R123	R124	R125	R126	Selection
0	0	No-pop	1K	No-pop	1K	AECLKIN *
0	1	No-pop	1K	1K	No-pop	CPU/4 Clock Rate
1	0	1K	No-pop	No-pop	1K	CPU/6 Clock Rate
1	1	1K	No-pop	1K	No-pop	Reserved

* default

1.8 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.2V or 1.4V and +3.3V using Texas Instruments voltage regulators. The +1.2V or 1.4V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug.

There are two power test points on the EVM at JP2 and JP3. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. Normally these jumpers are both closed. To measure the current passing through remove the jumpers and connect the pins with a current measuring device.

The EVM also provides +3.3V, supply for the daughter card. It is also possible to provide the daughter card with +12V and -12V when the optional external power connector is used.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320C6413/C6418 EVM.

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2.1 CPLD (Programmable Logic)

The C6413/C6418 EVM uses an Altera EPM3128TC100-10 Complex Programmable Logic Device (CPLD) device to implement:

- Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- SPI for LCD serial interface.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the EVM. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on theC6413/C6418 can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the EVM, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM3128TC100-10 is a 3.3V (5V tolerant), 100-pin QFP device that provides 128 macrocells, 80 I/O pins, and a 10 ns pin-to-pin delay. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the EVM). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the EVM on the installation CD-ROM.

2.1.2 CPLD Registers

The multiple CPLD memory-mapped registers allows users to control CPLD functions in software. On theC6413/C6418 EVM the registers are primarily used to access the LEDs and DIP switches, provide LCD interface, and control the daughter card interface. The registers are mapped into the EMIF data space at word address 0x900F010, in the upper portion of CE1. They appear as 8-bit registers with a simple 8-bit asynchronous memory interface. The following table gives a high level overview of the CPLD registers and their bit fields:

The table below shows the bit definitions for the 7 registers in CPLD.

Table 1: CPLD Register Definitions

Offset	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
1	DC_REG	DC_DET R	Reserved	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
2	Reserved								
3	Reserved								
4	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
5	Reserved								
6	MISC	McBSP0 On/Off R/W 0 (Onboard)	Reserved	Reserved	Reserved	Reserved	Reserved	McBSP2 ON/OFF Board R/W 0 (Onboard)	McBSP1 ON/OFF Board R/W 0 (Onboard)
7	Reserved								
8	LCD_REG0	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
9	LCD_REG1	SHIFT DATA7	SHIFT DATA6	SHIFT DATA5	SHIFT DATA4	SHIFT DATA3	SHIFT DATA2	SHIFT DATA1	SHIFT DATA0
A	BOARD	LCD Busy R 1 BUSY	LCD Reset R/W 0	Reserved R	Reserved R	SBRAM Enable R/W (0 Disabled)	Expansion I^2C Port 1 R/W (0 Off)	Expansion I^2C Port 0 R/W (0 Off)	Reserved

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the EVM. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch 3(1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch 2(1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch 1(1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch 0(1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the EVM and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	EVM_VER2	R	Most Significant EVM Board Version Bit
1	EVM_VER1	R	EVM Board Version Bit
0	EVM_VER0	R	Least Significant EVM Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On theC6413/C6418 EVM, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

McBSP0SEL, McBSP1SEL and McBSP2SEL control the McBSP0, McBSP1 and McBSP2 respectively. Usually these ports are used to interface ports to the on-board AIC23 codec, the RS-232 UART driver, or SPI Serial ROM as examples. The power-on state of these bits (both 0s) represents that situation. Setting the corresponding bit to 1 enables the McBSP to the expansion daughter-card instead interface.

Table 5: MISC Register

Bit	Name	R/W	Description
7	McBSP0SEL0	R/W	McBSP0 on/off board (0 = on-board, 1 = off-board)
6	Reserved	R	Reserved
5	Reserved	R	Reserved
4	Reserved	R	Reserved
3	Reserved	R	Reserved
2	Reserved	R	Reserved
1	MCBSP2SEL	R/W	McBSP2 on/off board (0 = on-board, 1 = off-board)
0	MCBSP1SEL	R/W	McBSP1 on/off board (0 = on-board, 1 = off-board)

2.1.7 LCD Interface

The Liquid Crystal Display (LCD) is a write only interface. It is interfaced via an 8-bit shift register.

Two locations are used when interfacing the LCD panel. Allowing the address bit of the interface to be directly programmed. The shift clock frequency is 5 megahertz.

Writing register LCD0 sets the LCD address line A0 to 0. Writing register LCD1 sets the LCD address line A0 to 1. The write operation to either of these locations starts an internal shift register serializing the data into an 8-bit sequence to the displays.

The table below shows the relationship of the DSP data bits to the LCD data bits.

Table 6: LCD Interface

D7	D6	D5	D4	D3	D2	D1	D0
LCD D7	LCD D6	LCD D5	LCD D4	LCD D3	LCD D2	LCD D1	LCD D0

The figure below shows the LCD data transfer timing. the CPLD automatically generates this timing.

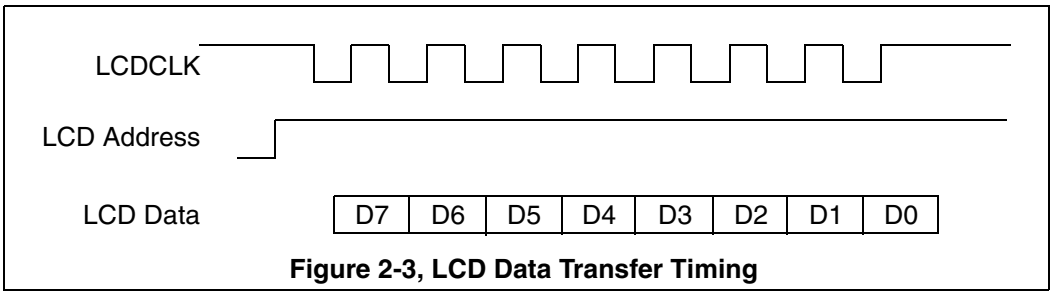


Figure 2-3, LCD Data Transfer Timing

After any write operations the CPLD sets the LCD BUSY bit in the C6413/C6418 EVM interface Register as the output is being serialized. The user should check this bit prior to starting another write operation. When LCD BUSY is high, the LCD shift register is busy, when is low the shift register is ready.

2.1.8 C6413/C6418 EVM Interface Register

The C6413/C6418 EVM Interface Register implements specific logic for the C6413/ C6418 EVM. The bits used in this register and their function are described in the table below.

Table 7: C6413/C6418 EVM Interface Register

Bit	Name	R/W	Description
7	LCD Busy	R	0 = busy, not ready, 1 = not busy, ready
6	LCD Reset	R/W	0 = removes reset from LCD, 1 = forces LCD into reset
5	Reserved		
4	Reserved		
3	SBRAM Disable	R/W	0 = SBRAM Enabled, 1 = SBRAM Disabled
2	I^2C Expansion Port 0	R/W	0 = Disables I^2C interface to expansion connector 1 = Enables I^2C interface to expansion connector
1	^2C Expansion Port 1	R/W	0 = Disables I^2C interface to expansion connector 1 = Enables I^2C interface to expansion connector
0	Reserved	R	

LCD Busy indicates the status of the CPLD implemented shift register which interfaces to the LCD panel. A 1 logic level indicates the shift register is busy, A 0 logic level indicates the shift register is ready.

LCD Reset allows the LCD Reset bit to be toggled under software control. A 1 logic level forces the LCD panel into reset. A 0 logic level removes the LCD reset to normal state.

SBRAM Enable determines if Chip Enable 3 is used to interface to the on board SBRAM or the daughter card interface. The default (logic 0) is that the SBRAM is enabled.

I^2C Expansion bit enables/disables driving the I^2C interface to the daughter card expansion bus. A 1 logic level enables the I^2C bus to the daughter card interface. A 0 logic level disables the interface. Default state is disabled.

2.2 AIC23 Codec

The EVM uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Codec interface on the C6413/C6418 EVM.

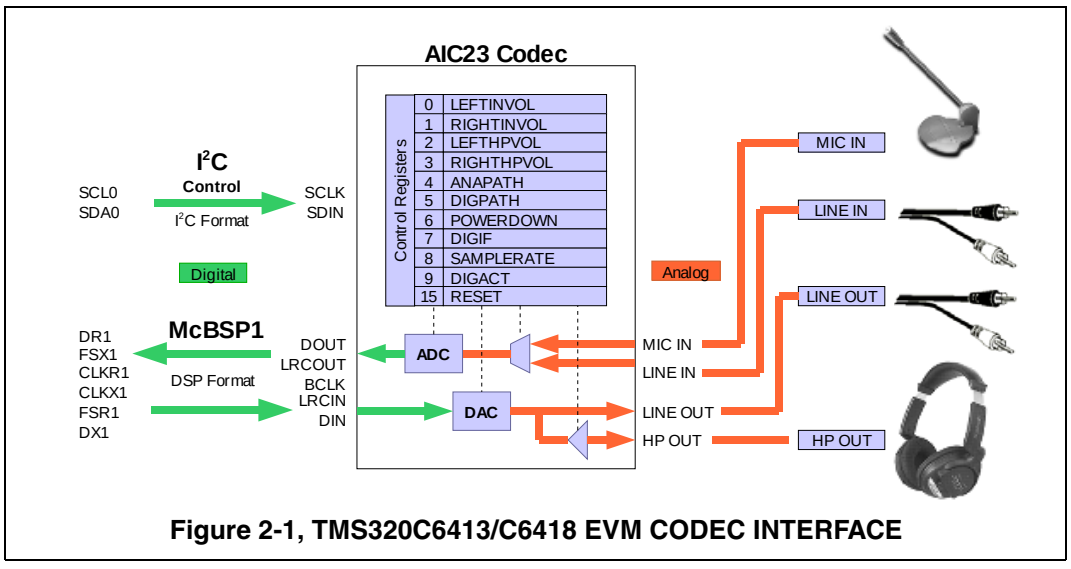


Figure 2-1, TMS320C6413/C6418 EVM CODEC INTERFACE

2.3 Synchronous DRAM

The EVM uses an industry standard 64 megabit Synchronous SDRAM. It uses a 32-bit interface and is used with up a maximum 100 MHz. memory clock. Since the DSP runs at 500 or 600 MHz, the EMIF must be programmed to use the SDRAM at a divider of the core clock rate or use the alternate EMIF Clock input.

The SDRAM occupies chip enable 0.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

2.4 Flash Memory

The EVM provides two devices each consisting of 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M 32 bit words. Typically the Flash is mapped into CE1 space because that is where the bootloader looks for a boot image when booting from the Flash. Because the bootloader default configuration is 8 bit boot mode usually only the Flash on D0-D7 is used. The CE1 space is shared by the CPLD, UART, and the Flash, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 80ns, and typically 100 ns.

2.5 SBRAM Memory

The EVM has 1 megabyte of SBRAM optionally mapped in CE3 space. If the SBRAM is not used CE3 can be used for expansion daughter card accesses by disabling the secondary chip select on the SBRAM via the Board Register in the CPLD.

2.6 LEDs and DIP Switches

The EVM includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.7 Daughter Card Interface

The EVM provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and the Host Port Interface (HPI)

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundries. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

The HPI is a high speed interface that can be used to allow multiple DSPs to communicate and cooperate on a given task. The HPI connector brings out the HPI specific control signals as well as McBSP2.

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the EVM board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The EVM also multiplexes the Mc_BSP0, McBSP1, and McBSP2 for on-board or external use. This function is controlled through the CPLD MISC register.

The timer signals on the peripheral expansion connector have connections for both inputs and outputs. These map to the TIN and TOUT pins on the C6413/C6418 device.

2.8 TL16C550 UART

The C6413/C6418 EVM has an on board TLC16C550 UART. The UART is buffered with a SN75LV4737A RS-232 line driver and is routed to a male 9 pin D-connector, P4. The pin positions for the P4 connector as viewed from the edge of the printed circuit board are shown below.

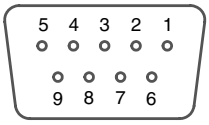


Figure 3-9, P4, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 8: P4, RS-232 Pinout

Pin #	Target Signal Name	Target Direction
1	Reserved	Not Used
2	TXD	Out
3	RXD	In
4	DSR	In
5	GND	N/A
6	DTR	Out
7	CTS	In
8	RRTS	Out
9	Reserved	Not Used

The UART occupies 8 locations mapped at address 0x900F0000 - 0x900F000F in CE1 space with the EMIF in 8 bit synchronous memory mode. The UART uses the NMI interrupt for interrupt based communication.

Chapter 3

Physical Description

This chapter describes the physical layout of the TMS320C6413/C6418 EVM and its connectors.

Topic **Page**

3.1 TMS320C6413/C6418 EVM Board Layout

The C6413/C6418 EVM is a 8.25 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. The figure below shows the layout of the C6413/C6418 EVM.

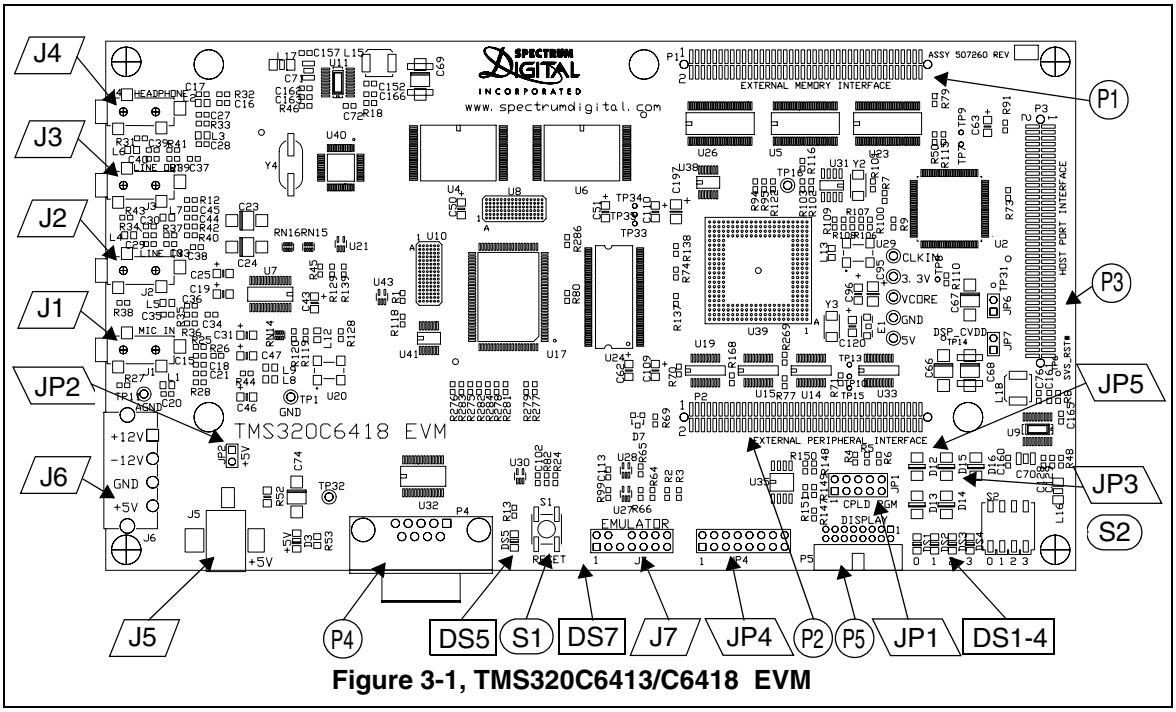


Figure 3-1, TMS320C6413/C6418 EVM

3.2 Keypad/display Module Layout

The Keypad/display Module is a 3.1 x 4.4 inch (79 x 112 mm.) multi-layer board which is powered from the EVM. The figure below shows the layout of the Keypad/display Module.

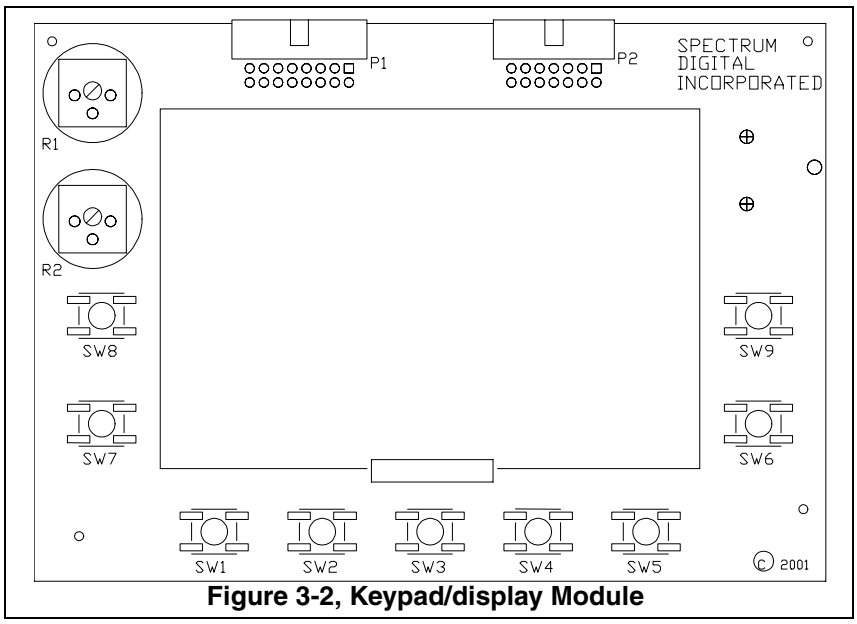


Figure 3-2, Keypad/display Module

3.3 Connector Index

The TMS320C6413/C6418 EVM has many connectors which provide the user access to the various signals on the EVM.

Table 1: TMS320C6413/C6418 EVM Connectors

Connector	# Pins	Function
P1	80	Memory
P2	80	Peripheral
P3	80	HPI
P4	9	RS-232 Port
P5	16	Display - Keypad
J1	2	Microphone
J2	2	Line In
J3	2	Line Out
J4	2	Speaker
J5	2	+5 Volt
J6 *	4	Alternate Power Connector
J7	14	External JTAG

Note: **"*"** Not populated

3.4 Expansion Connectors

The TMS320C6413/C6418 EVM supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

The three expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the EVM. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the EVM. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card, if the alternate power supply connector is used to power the board. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: I is on an Input pin
O is on an Output pin
Z is on a High Impedance pin

3.4.1 P1, Memory Expansion Connector

Table 2: P1, Memory Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+5 Volts	O	2	+5 volts	O
3	A21	O	4	A20	O
5	A19	O	6	A18	O
7	A17	O	8	A16	O
9	A15	O	10	A14	O
11	GND	O	12	GND	O
13	A13	O	14	A12	O
15	A11	O	16	A10	O
17	A9	O	18	A8	O
19	A7	O	20	A6	O
21	+5 Volts	O	22	+5 Volts	O
23	A5	O	24	A4	O
25	A3	O	26	A2	O
27	BE3n	O	28	BE2n	O
29	BE1n	O	30	BE0n	O
31	GND	O	32	GND	O
33	D31	I/O/Z	34	D30	I/O/Z
35	D29	I/O/Z	36	D28	I/O/Z
37	D27	I/O/Z	38	D26	I/O/Z
39	D25	I/O/Z	40	D24	I/O/Z
41	+3.3 Volts	O	42	+3.3 Volts	O
43	D23	I/O/Z	44	D22	I/O/Z
45	D21	I/O/Z	46	D20	I/O/Z
47	D19	I/O/Z	48	D18	I/O/Z
49	D17	I/O/Z	50	D16	I/O/Z
51	GND	O	52	GND	O
53	D15	I/O/Z	54	D14	I/O/Z
55	D13	I/O/Z	56	D12	I/O/Z
57	D11	I/O/Z	58	D10	I/O/Z
59	D9	I/O/Z	60	D8	I/O/Z
61	GND	O	62	GND	O
63	D7	I/O/Z	64	D6	I/O/Z
65	D5	I/O/Z	66	D4	I/O/Z
67	D3	I/O/Z	68	D2	I/O/Z
69	D1	O	70	D0	O
71	GND	O	72	GND	O
73	REn	O	74	WEn	O
75	OEn	O	76	RDYn	I
77	CE3n	O	78	CE2n	O
79	GND	O	80	GND	O

3.4.2 P2, Peripheral Expansion Connector

Table 3: P2, Peripheral Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+12 Volts *	O	2	-12 Volts *	O
3	GND	O	4	GND	O
5	+5 Volts	O	6	+5 Volts	O
7	GND	O	8	GND	O
9	+5 Volts	O	10	+5 Volts	O
11	* I^2C SCL1	O/Z	12	* I^2C SDA1	I/O/Z
13	RESERVED		14	RESERVED	
15	RESERVED		16	RESERVED	
17	RESERVED		18	RESERVED	
19	+3.3 Volts	O	20	+3.3 Volts	O
21	CLKX0	I/O/Z	22	CLKS0	
23	FSX0	I/O/Z	24	DX0	O/Z
25	GND	O	26	GND	O
27	CLKR0	I/O/Z	28	RESERVED	
29	FSR0	I/O/Z	30	DR0	I
31	GND	O	32	GND	O
33	CLKX1	I/O/Z	34	CLKS1	I
35	FSX1	I/O/Z	36	DX1	O/Z
37	GND	O	38	GND	O
39	CLKR1	I/O/Z	40	RESERVED	
41	FSR1	I/O/Z	42	DR1	Z
43	GND	O	44	GND	O
45	TOUT0	Z	46	TIN0	I
47	INT0n	I	48	INT5n	I
49	TOUT1	O	50	TIN1	I
51	GND	O	52	GND	O
53	INT4n	I	54	IACKn	I
55	RESERVED		56	INT7n	O
57	RESERVED		58	RESERVED	I
59	RESETn	O	60	RESERVED	
61	GND	O	62	GND	O
63	DC_CNTL1	O	64	DC_CNTL0	O
65	DC_STAT1	I	66	DC_STAT0	I
67	INT6n	I	68	RESERVED	
69	RESERVED		70	RESERVED	
71	RESERVED		72	RESERVED	
73	RESERVED		74	RESERVED	
75	DETECTn	I	76	GND	O
77	GND	O	78	CLKOUT	O
79	GND	O	80	GND	O

* Enable via CPLD Bit

3.4.3 P3, HPI Expansion Connector

Table 4: P3, HPI Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	Reserved	O	2	+5 Volts	O
3	GND	I/O/Z	4	HPI_RESET	I/O/Z
5	GP0	I/O/Z	6	GP3	I/O/Z
7	HD30	O/Z	8	HD31	I
9	GND	I/O	10	GND	I
11	HD28/AMUTE1	O	12	HD29/AMUTEIN1	O
13	HD26/AHCHKR1	I	14	HD27/AHCLKX1	I
15	HD24/ACLKX1	I	16	HD25/ACLKR1	I
17	HD22/AFSX1	I/O	18	HD23/AFSR1	I/O
19	GND	I	20	GND	I
21	HD20/AXR1[4]	O	22	HD21/AXR1[5]	O
23	HD18/AXR1[2]	O/Z	24	HD19/AXR1[3]	O/Z
25	HD16/AXr1[0]	I	26	HD17/AXR1[1]	I
27	HD14/GP14	I	28	HD15/GP15	I
29	GND	I	30	GND	I
31	HD12/GP12	O	32	HD13/GP13	O
33	HD10/GP10	I	34	HD11/GP11	I
35	HD8/GP8	I	36	HD9/GP9	I
37	HD6	I	38	HD7	I
39	GND	I	40	GND	I
41	HD4	O	42	HD5	O
43	HD2	I	44	HD3	I
45	HD0	I	46	HD1	I
47	HCTL1/EATCLK	I	48	HRDY/ATCLK	I
49	GND	I	50	GND	I
51	HAS/ACLKR1[1]	O	52	HINT/MODCLK	O
53	HCS/ACLKR1[2]	I/O/Z	54	HCTL0/AFSR1[1]	I/O/Z
55	HDS1/ACLKR1[3]	I/O/Z	56	HWIL/AFSR1[2]	I/O/Z
57	HDS2	I/O/Z	58	HRW/AFSR1[3]	I/O/Z
59	GND	I/O/Z	60	GND	I/O/Z
61	AXR0[2]	O	62	AXR0[0]	O
63	AXR0[4]	I/O/Z	64	AXR0[1]	I/O/Z
65	AXR0[5]	I/O/Z	66	AXR0[3]	I/O/Z
67	AHCLKX0	I/O/Z	68	I^2C SCL0	I/O/Z
69	ACLKX0	I/O/Z	70	GND	I/O/Z
71	AHCLKR0	O	72	I^2C SDA0	O
73	ACLKR0	O/Z	74	GND	I
75	AFSR0	I	76	AMUTE0	I/O
77	AFSX0	O	78	AMUTEIN0	I
79	GND	O	80	GND	O

3.5 Audio Connectors

The C6413/C6418 EVM has 4 audio connectors. They are described in the following sections.

3.5.1 J1, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

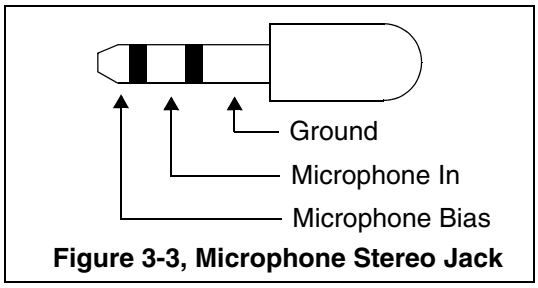


Figure 3-3, Microphone Stereo Jack

3.5.2 J2, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

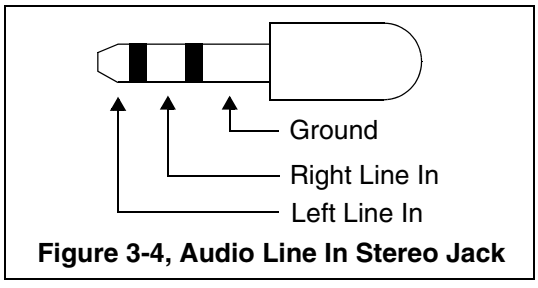


Figure 3-4, Audio Line In Stereo Jack

3.5.3 J3, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

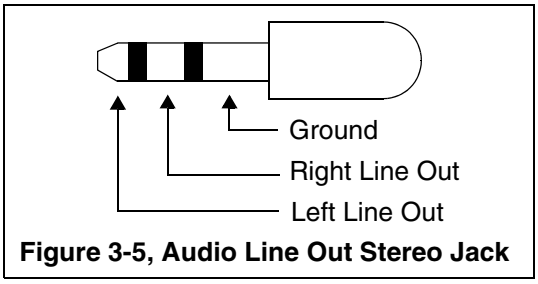


Figure 3-5, Audio Line Out Stereo Jack

3.5.4 J4, Headphone Connector

Connector J4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below

.

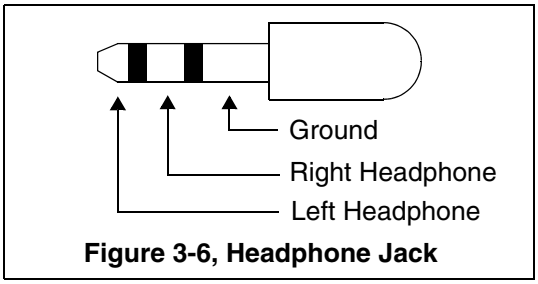


Figure 3-6, Headphone Jack

3.6 Power Connectors

The C6413/C6418 EVM has 2 power connectors. They are described in the following sections.

3.6.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320C6413/C6418 EVM via the J5 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.

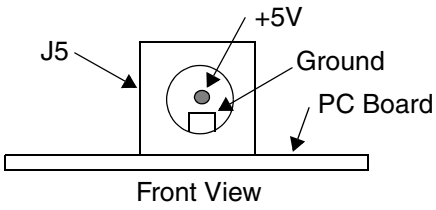


Figure 3-7, TMS320C6413/C6418 EVM Power Connector

3.6.2 J6, Alternate Power Connector

Connector J6 is an alternate power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #53109-0410. The table below shows the voltages on the respective pins.

Table 5: J6, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

3.7 Miscellaneous Connectors

The C6413/C6418 EVM has 3 additional connectors to aid the user in developing with this product. They are described in the following sections.

3.7.1 P4, RS-232 Connector

Connector P4 is a female RS-232 providing an interface to the UART. The signals on this connector are shown in the below.

Table 6: P4, RS-232 Connector

Pin #	Signal Name	Direction
1	Reserved	
2	Transmit Data	Output
3	Receive Data	Input
4	Reserved	
5	Ground	Output
6	Reserved	
7	CTS	Input
8	RTS	Output
9	Reserved	

3.7.2 J7, External JTAG Connector

The TMS320C6413/C6418 EVM is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

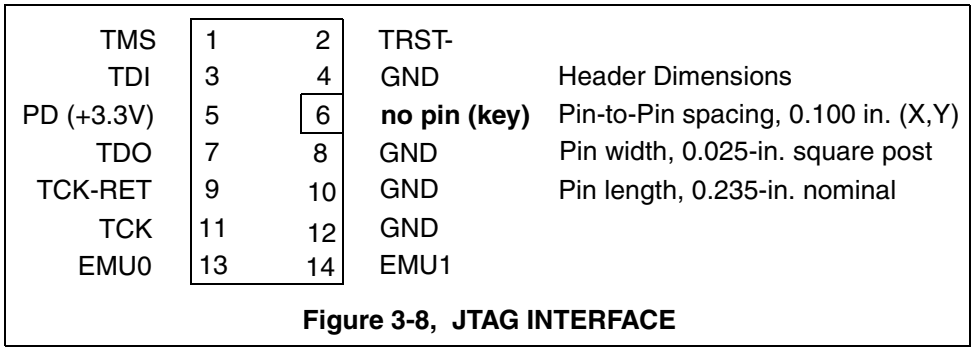


Figure 3-8, JTAG INTERFACE

3.7.3 JP1, PLD Programming Connector

This connector interfaces to the Altera CPLD, U2. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

3.8 P5, Keypad/Display Connector

The EVM supports a 16 pin 2 mm. connector which interfaces to the keypad/display unit. The signals on the 8 x 2 connector are shown in the table below.

Table 7: System LEDs

Pin #	Signal	Pin #	Signal
1		2	1
3		4	1
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	

3.9 System LEDs

TheTMS320C6413/C6418 EVM has two system light emitting diodes (LEDs). These LEDs indicate various conditions on the EVM. These function of each LED is shown in the table below.

Table 8: System LEDs

Reference Designator	Color	Function	On Signal State
DS6	Green	+5 Volt present	1
DS5	Orange	RESET Active	1

3.10 Reset Circuitry

There are three resets on the TMS320C6413/C6418 EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C6413/C6418.

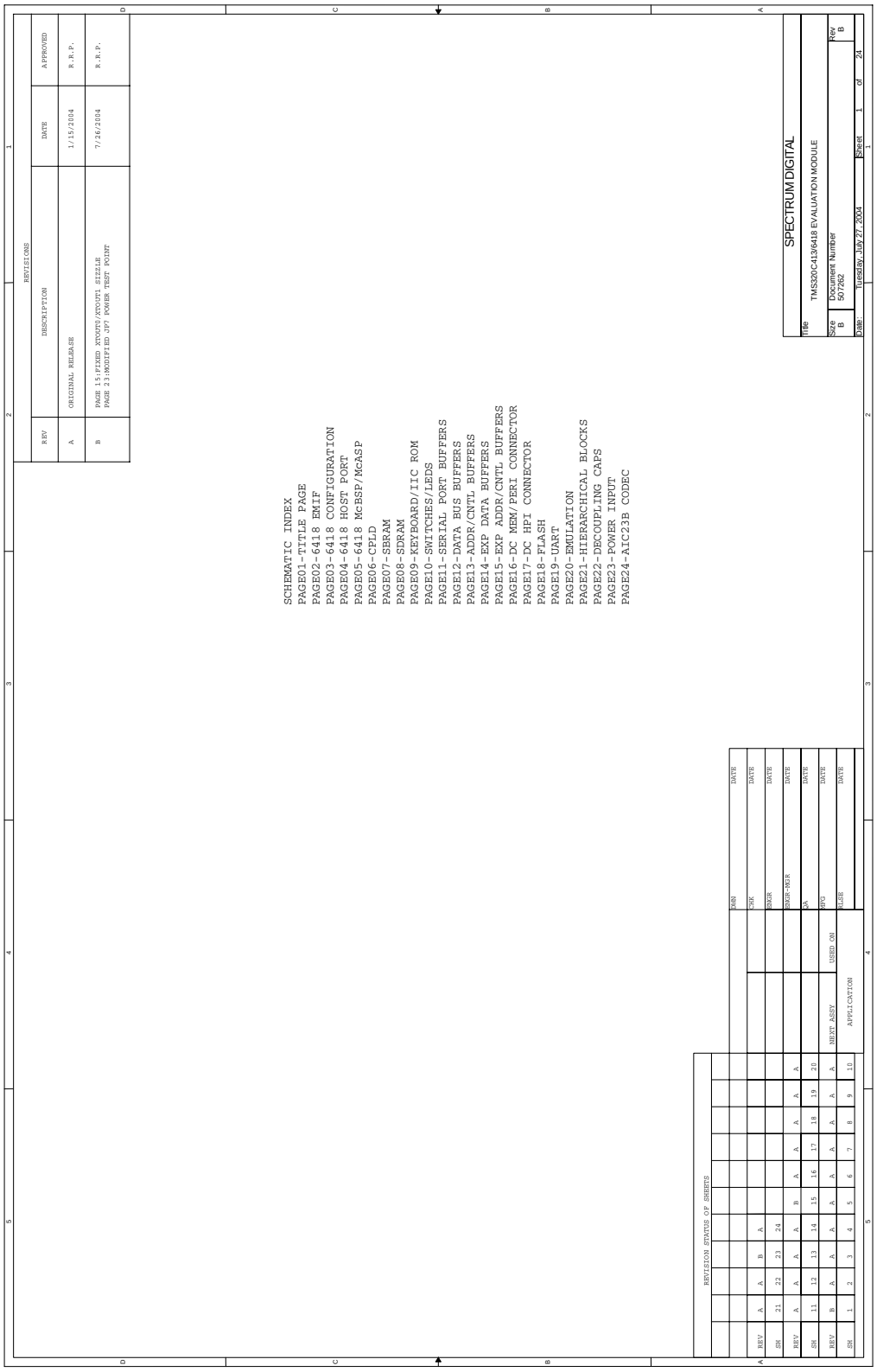
External sources which control the reset are push button S1, and HPI Reset from the expansion connector.

Appendix A

Schematics

This appendix contains the schematics for the TMS320C6413/C6418 EVM and the keypad/display module.

Topic **Page**



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ORIGINAL RELEASE	1/15/2004	R.R.P.
B	PAGE 15: FIXED XTOUT0/XTOUT1 SIZZLE PAGE 23:MODIFIED OFF POWER TEST POINT	7/26/2004	R.R.P.

SCHEMATIC INDEX
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PAGE02-6418 EMIF
PAGE03-6418 CONFIGURATION
PAGE04-6418 HOST PORT
PAGE05-6418 McBSP/McASP
PAGE06-CPLD
PAGE07-SBRAM
PAGE08-SDRAM
PAGE09-KEYBOARD/IIC ROM
PAGE10-SWTCHES/LEDS
PAGE11-SERIAL PORT BUFFERS
PAGE12-DATA BUS BUFFERS
PAGE13-ADDR/CNTL BUFFERS
PAGE14-EXP DATA BUFFERS
PAGE15-EXP ADDR/CNTL BUFFERS
PAGE16-DC MEM/PERI CONNECTOR
PAGE17-DC HPI CONNECTOR
PAGE18-FLASH
PAGE19-UART
PAGE20-EMULATION
PAGE21-HIERARCHICAL BLOCKS
PAGE22-DECOUPLING CAPS
PAGE23-POWER INPUT
PAGE24-AIC23B CODEC

REVISION STATUS OF SHEETS

SH	1	2	3	4	5	6	7	8	9	10
REV	B	A	A	A	A	A	A	A	A	A

SH	11	12	13	14	15	16	17	18	19	20
REV	A	A	A	A	B	A	A	A	A	A

SH	21	22	23	24
REV	A	A	A	A

APPLICATION
NEXT ASSY USED ON

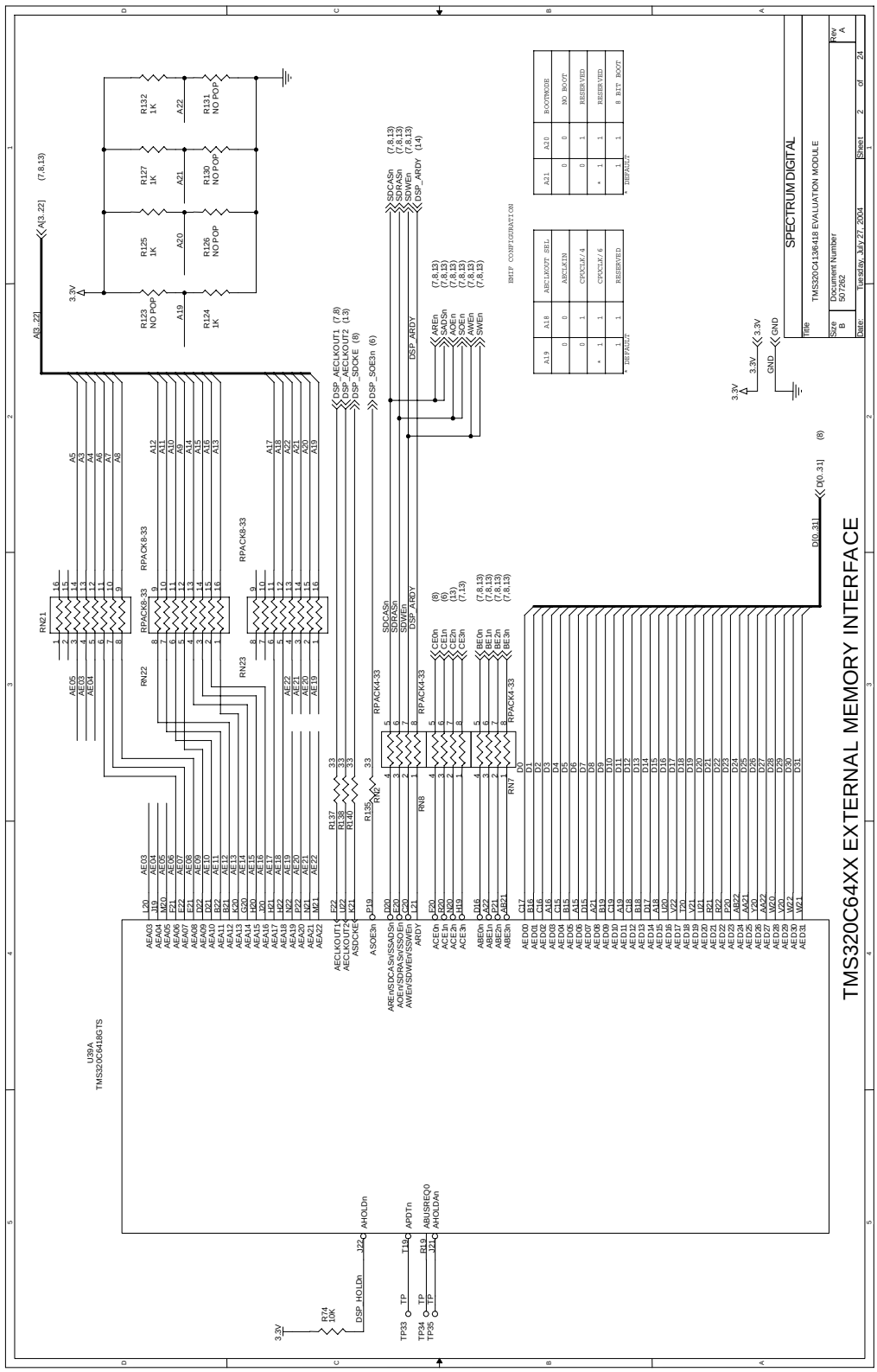
DRAWN	DATE
CHK	DATE
ENGR	DATE
ENGR MGR	DATE
QA	DATE
APVD	DATE
RELEASE	DATE

SPECTRUM DIGITAL

Title: TMS320C413/6418 EVALUATION MODULE

Size	Document Number	Rev
B	507262	B

Date: Tuesday, July 27, 2004 Sheet 1 of 24


TMS320C64XX EXTERNAL MEMORY INTERFACE
SPECTRUM DIGITAL
TMS320C/C1364/418 EVALUATION MODULE
Document Number
501282
Tuesday, July 27, 2004
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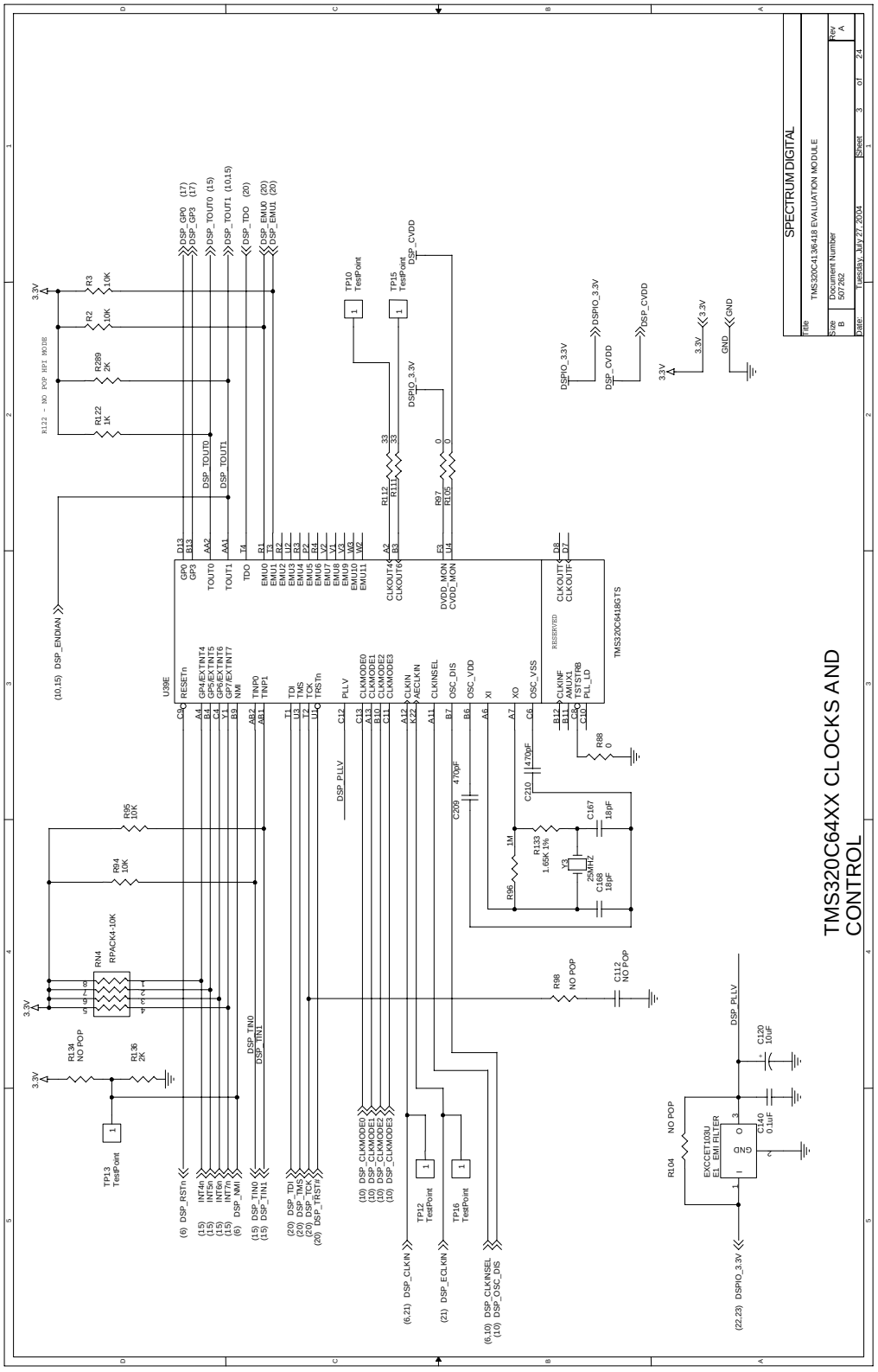
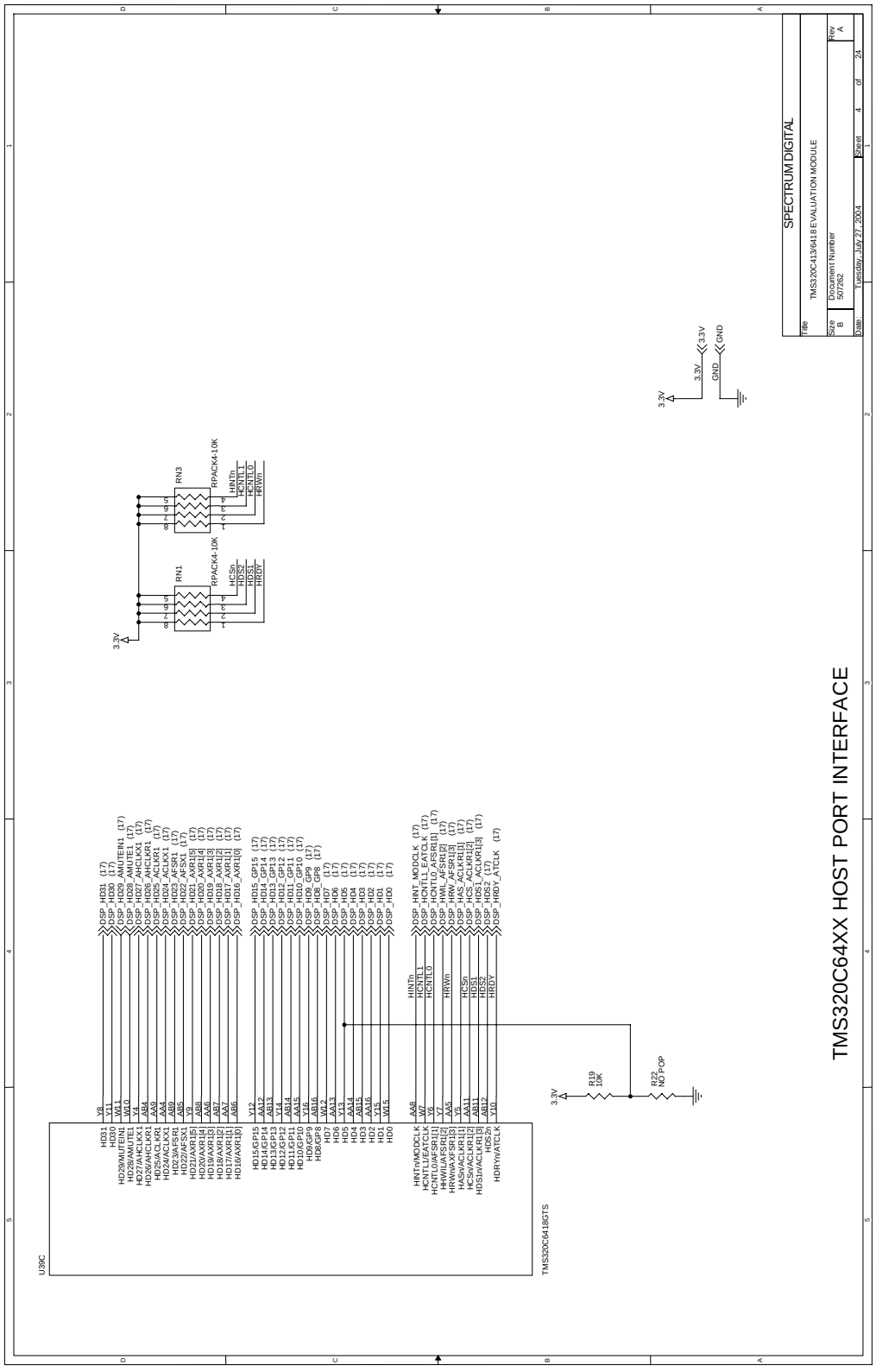
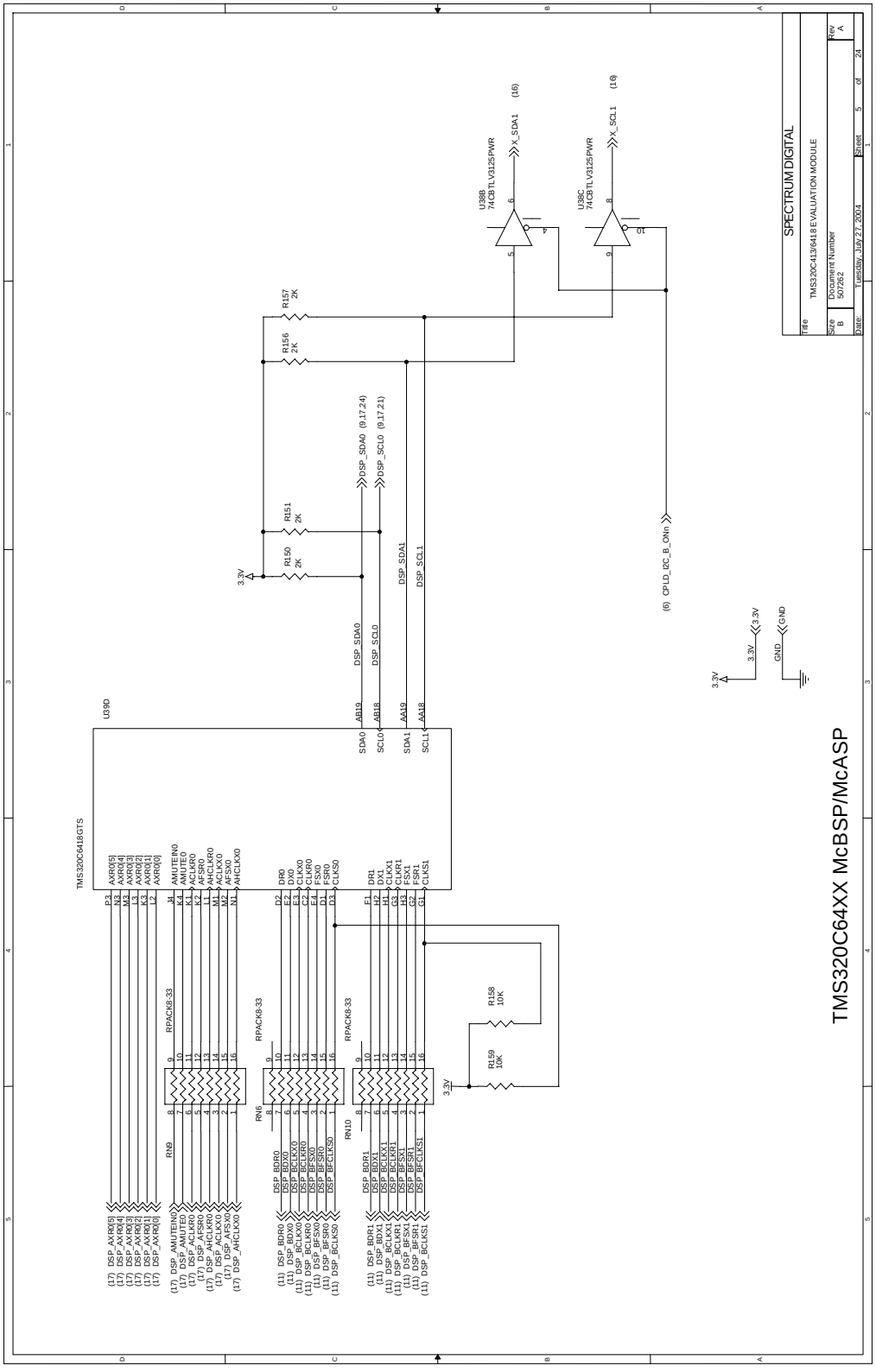
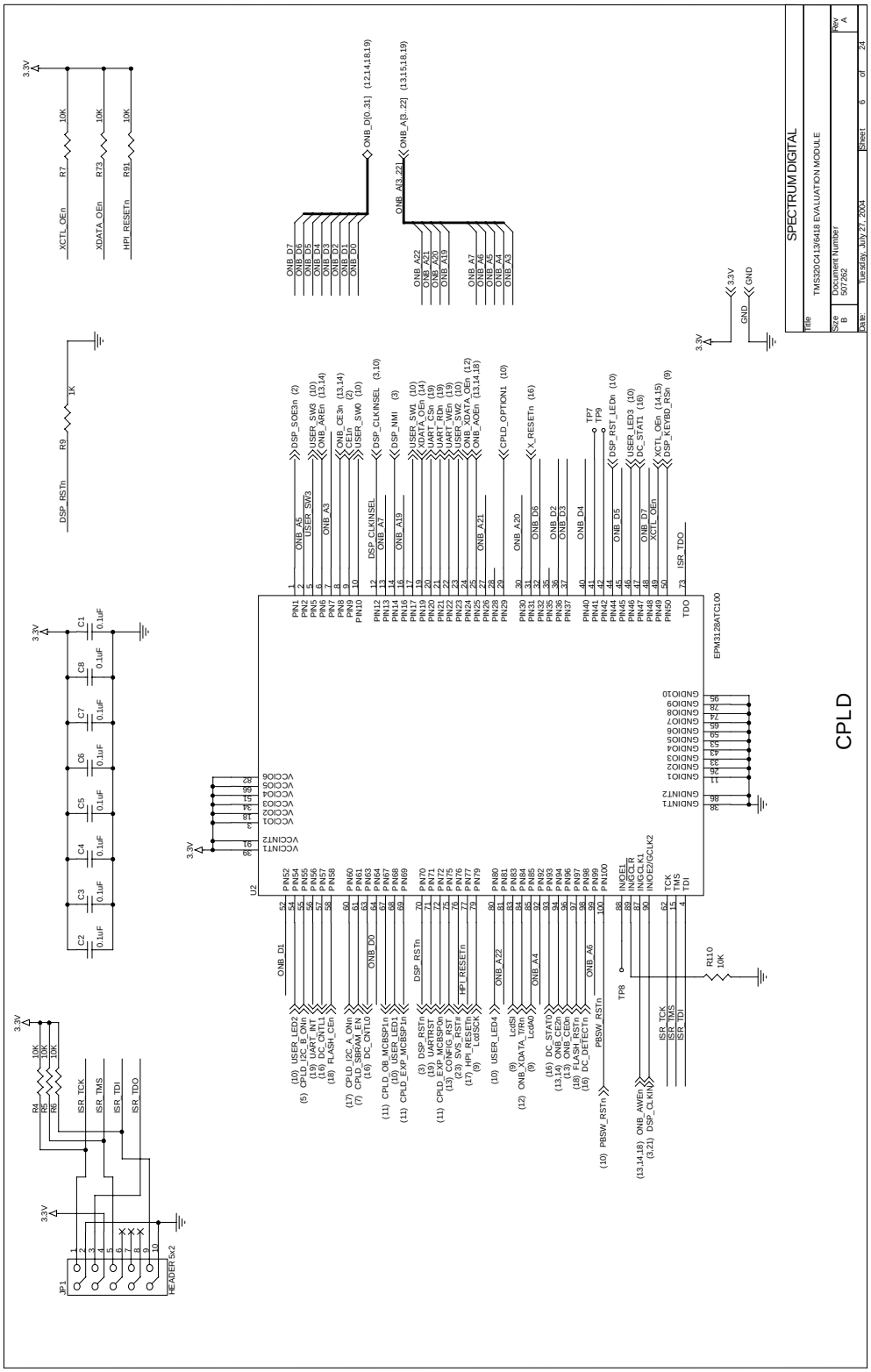
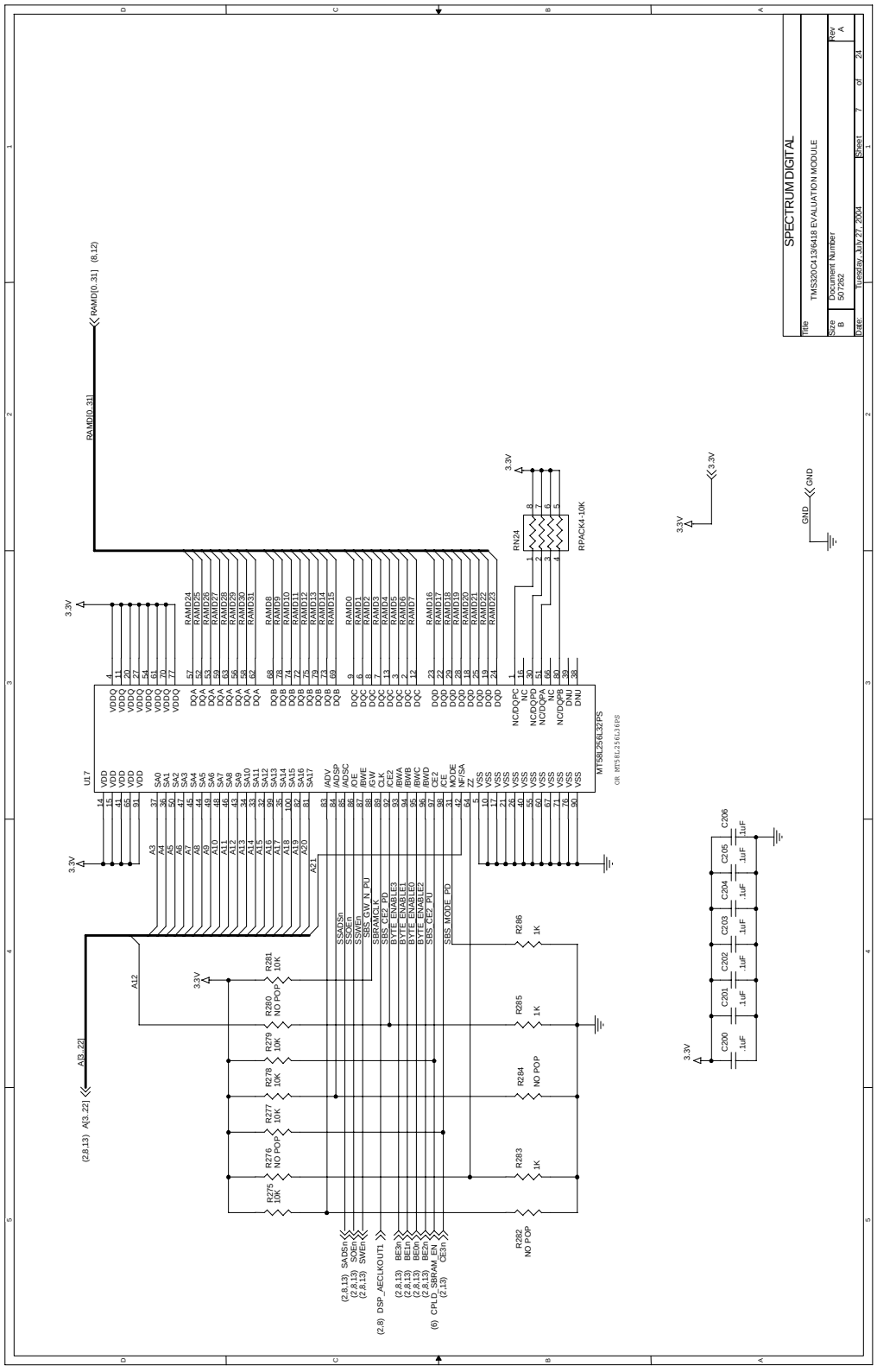
U39A
TMS320C6418GTS
BMIF CONFIGURATION
A19 A18 ABCLKOUT SEL
A21 A20 BOOTMODE
NO BOOT
RESERVED
CPUCLK/4
CPUCLK/6
B BIT BOOT
* DEFAULT
RN21
RN22
RN23
RN8
RN7
RPACK8-33
RPACK4-33
R123 NO POP
R124 1K
R125 1K
R126 NO POP
R127 1K
R130 NO POP
R131 NO POP
R132 1K
R74 10K
TP33
TP34
TP35
3.3V
GND
DSP_HOLDn
AHOLDn
APDTn
ABUSREQ0
AHOLDAn
A[3..22] (7,8,13)
D[0..31] (8)
DSP_ARDY
DSP_SOE3n (6)
DSP_SDCKE (8)
DSP_AECLKOUT1 (7,8)
DSP_AECLKOUT2 (13)
SDCASn (7,8,13)
SDRASn (7,8,13)
SDWEn (7,8,13)
DSP_ARDY (14)
AREn (7,8,13)
SSOEn (7,8,13)
AOEn (7,8,13)
SOEn (7,8,13)
AWEn (7,8,13)
SWEn (7,8,13)
CE0n (8)
CE1n (8)
CE2n (13)
CE3n (7,13)
BE0n (7,8,13)
BE1n (7,8,13)
BE2n (7,8,13)
BE3n (7,8,13)

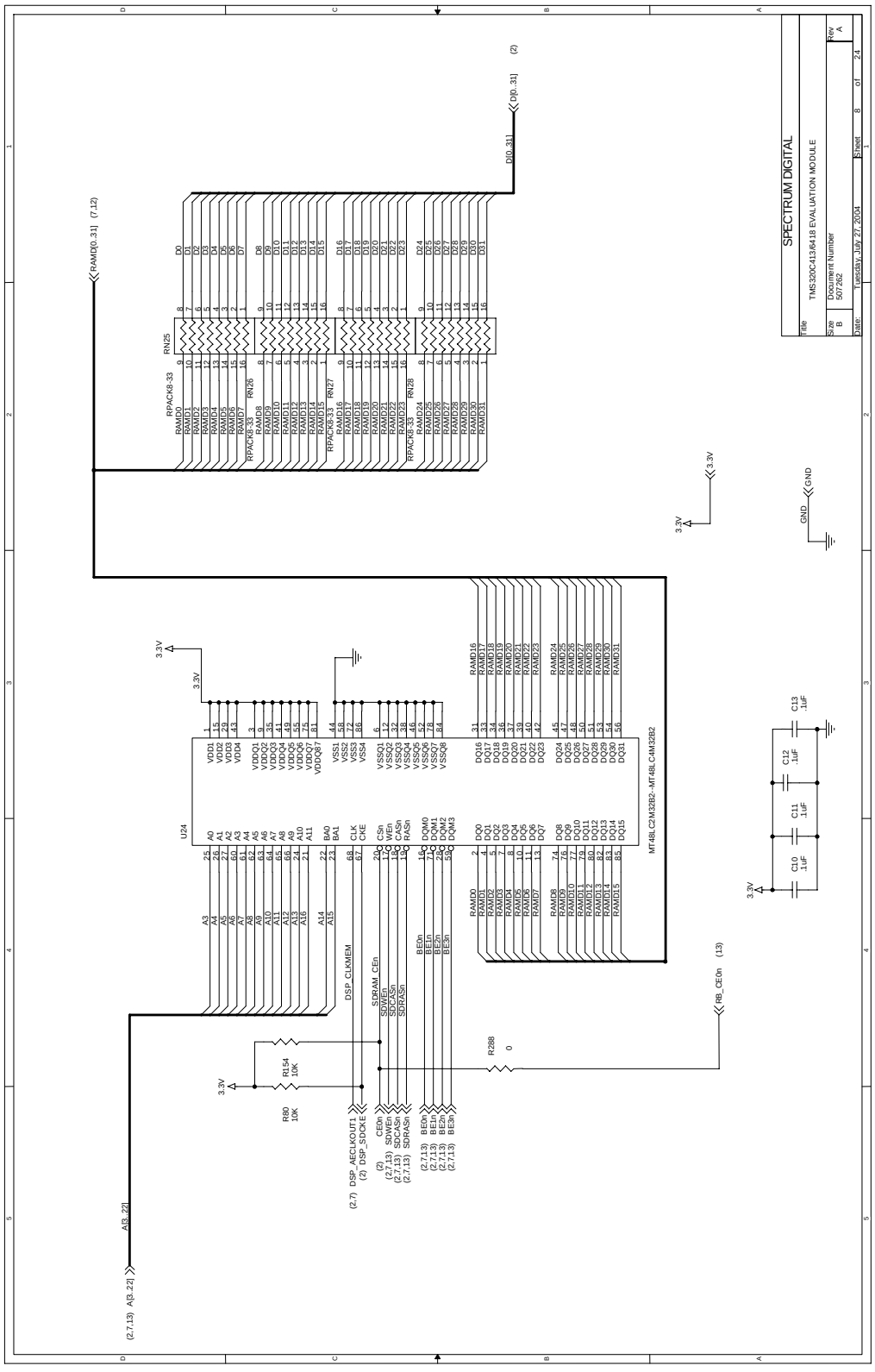

TMS320C64XX CLOCKS AND CONTROL
SPECTRUM DIGITAL
TMS320C41364418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
TMS320C64418GTS
U39E
RESETn
GP0
GP3
GP4/EXTINT4
GP5/EXTINT5
GP6/EXTINT6
GP7/EXTINT7
NMI
TOUT0
TOUT1
TDO
EMU0
EMU1
EMU2
EMU3
EMU4
EMU5
EMU6
EMU7
EMU8
EMU9
EMU10
EMU11
TINP0
TINP1
TDI
TMS
TCK
TRSTn
PLLV
CLKMODE0
CLKMODE1
CLKMODE2
CLKMODE3
CLKIN
AECLKIN
CLKINSEL
OSC_DIS
OSC_VDD
XI
XO
OSC_VSS
CLKOUT4
CLKOUT6
DVDD_MON
CVDD_MON
RESERVED
CLKOUT8
CLKOUTF
CLKINF
AUX1
TSTSTRB
PLL_LD
DSP_PLLV
DSP_CVDD
DSPIO_3.3V
3.3V
GND
R95 10K
R94 10K
RN4 RPACK4-10K
R134 NO POP
R135 2K
R22 1K
R289 2K
R2 10K
R3 10K
R112 33
R111 33
R97 0
R105 0
R88 0
R98 NO POP
C112 NO POP
C209 470pF
C210 470pF
R96 1M
R133 1.65K 1%
Y3 25MHZ
C167 18pF
C168 18pF
R104 NO POP
EXCCET103U E1_EMI FILTER
C120 10uF
C140 0.1uF
TP10 TestPoint
TP15 TestPoint
TP13 TestPoint
TP12 TestPoint
TP16 TestPoint
R122 - NO POP HPI MODE
DSP_ENDIAN
DSP_GP0
DSP_GP3
DSP_TOUT0
DSP_TOUT1
DSP_TDO
DSP_EMU0
DSP_EMU1
DSP_TIN0
DSP_TIN1
DSP_RSTn
DSP_NMI
DSP_TDI
DSP_TMS
DSP_TCK
DSP_TRST#
DSP_CLKIN
DSP_ECLKIN
DSP_CLKINSEL
DSP_OSC_DIS

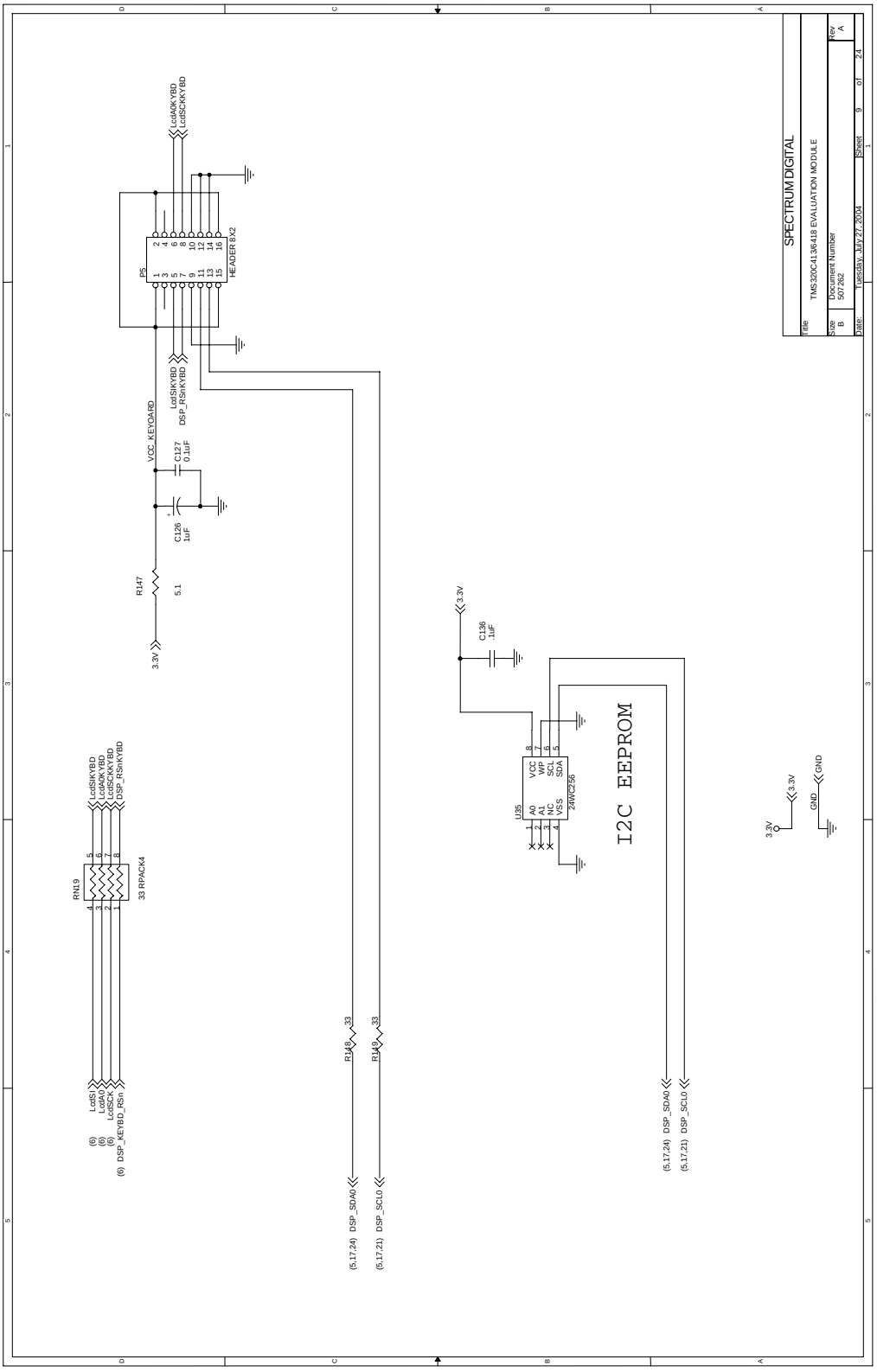

TMS320C64XX HOST PORT INTERFACE
SPECTRUM DIGITAL
TMS320C6413/6418 EVALUATION MODULE
Document Number
507362
Tuesday, July 27, 2004
U39C
TMS320C6418GTS
RN1
RN3
RPACK4-10K
R19
10K
R22
NOPOP
3.3V
GND

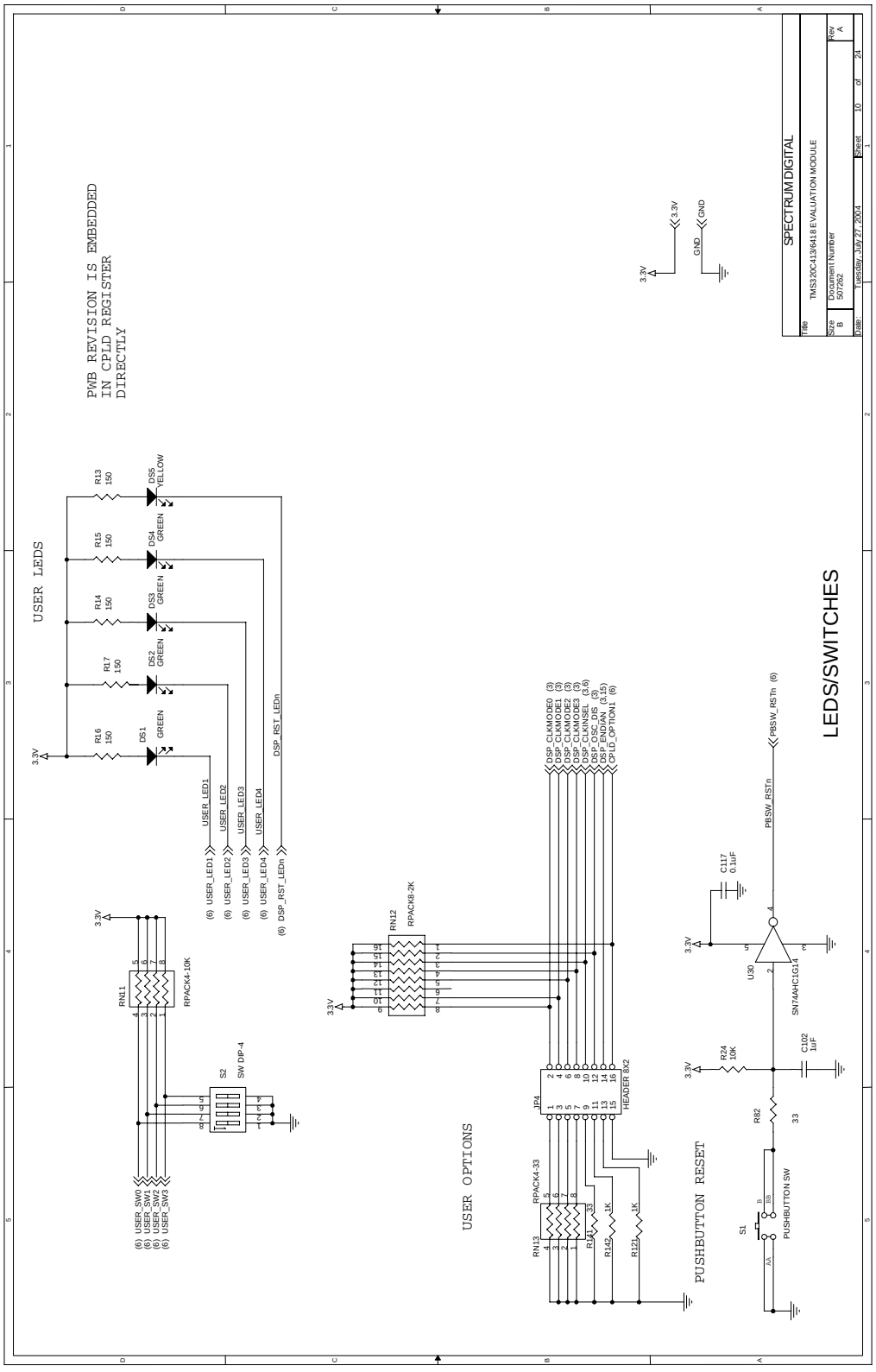

TMS320C64XX McBSP/McASP
SPECTRUM DIGITAL
TMS320C6418GTS
U39D
U39B
74CB3TLV3125PWR
U39C
74CB3TLV3125PWR
X_SDA1
X_SCL1
DSP_SDA0
DSP_SCL0
DSP_SDA1
DSP_SCL1
R150 2K
R151 2K
R156 2K
R157 2K
R158 10K
R159 10K
RN6
RN8
RN10
RPACK8-33
3.3V
GND

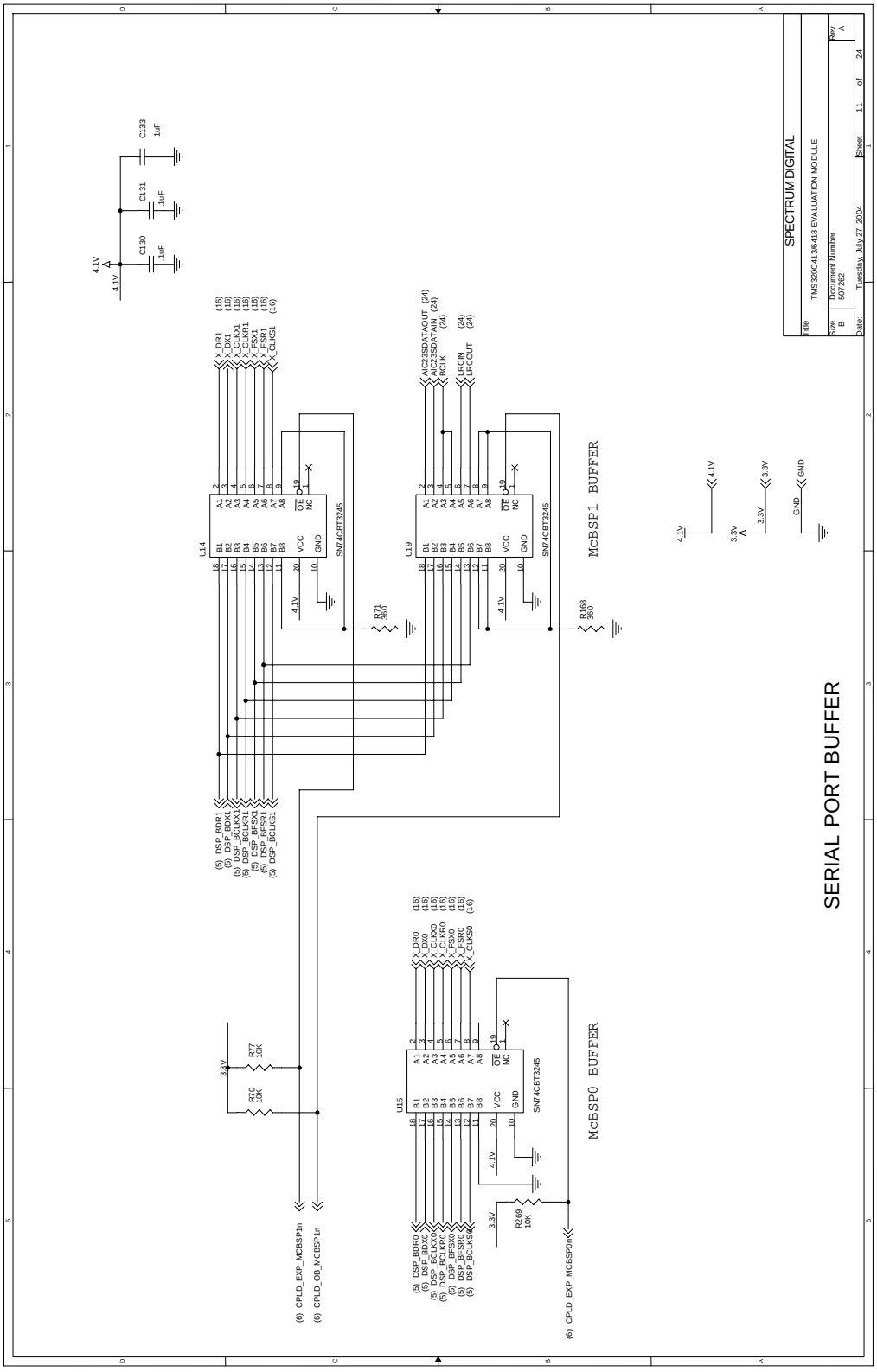

CPLD
SPECTRUM DIGITAL
TMS320C6713/6418 EVALUATION MODULE
Document Number 507262
Rev A
Sheet 6 of 24
Tuesday, July 27, 2004
EPM3128ATC100
U2
JP1
HEADER 5x2
R4 10K
R5 10K
R6 10K
R9 1K
R110 10K
R7 10K
R73 10K
R91 10K
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
XCTL_OEn
XDATA_OEn
HPI_RESETn
DSP_RSTn
ONB_D[0..31] (12,14,18,19)
ONB_A[3..22] (13,15,18,19)
ISR_TCK
ISR_TMS
ISR_TDI
ISR_TDO
TCK
TMS
TDI
TDO

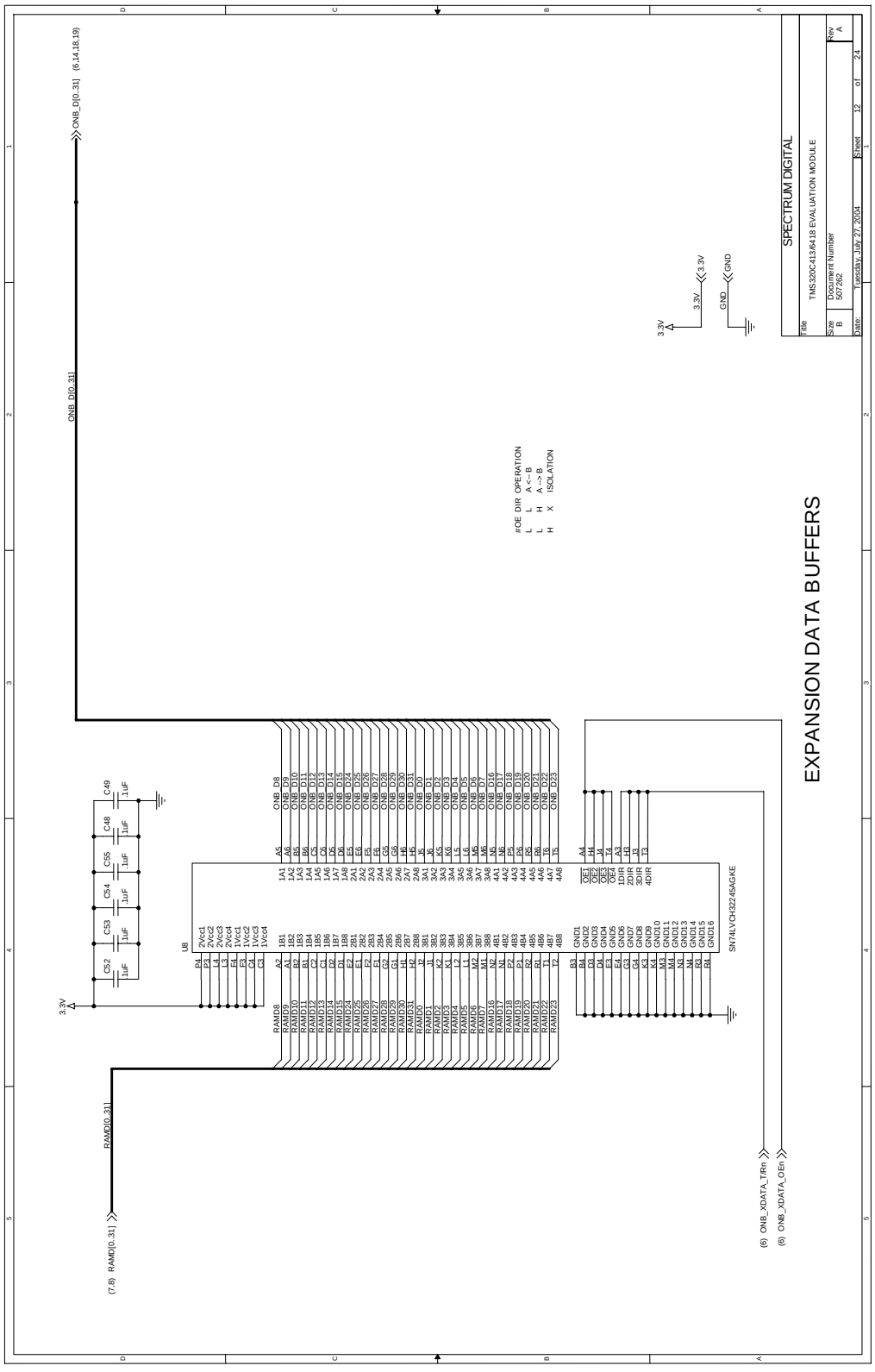

SPECTRUM DIGITAL
TMS320C413/6418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
U17
MT58L256L32PS
RN24
RPACK4-10K
RAMD[0..31]
A[3..22]
3.3V
GND

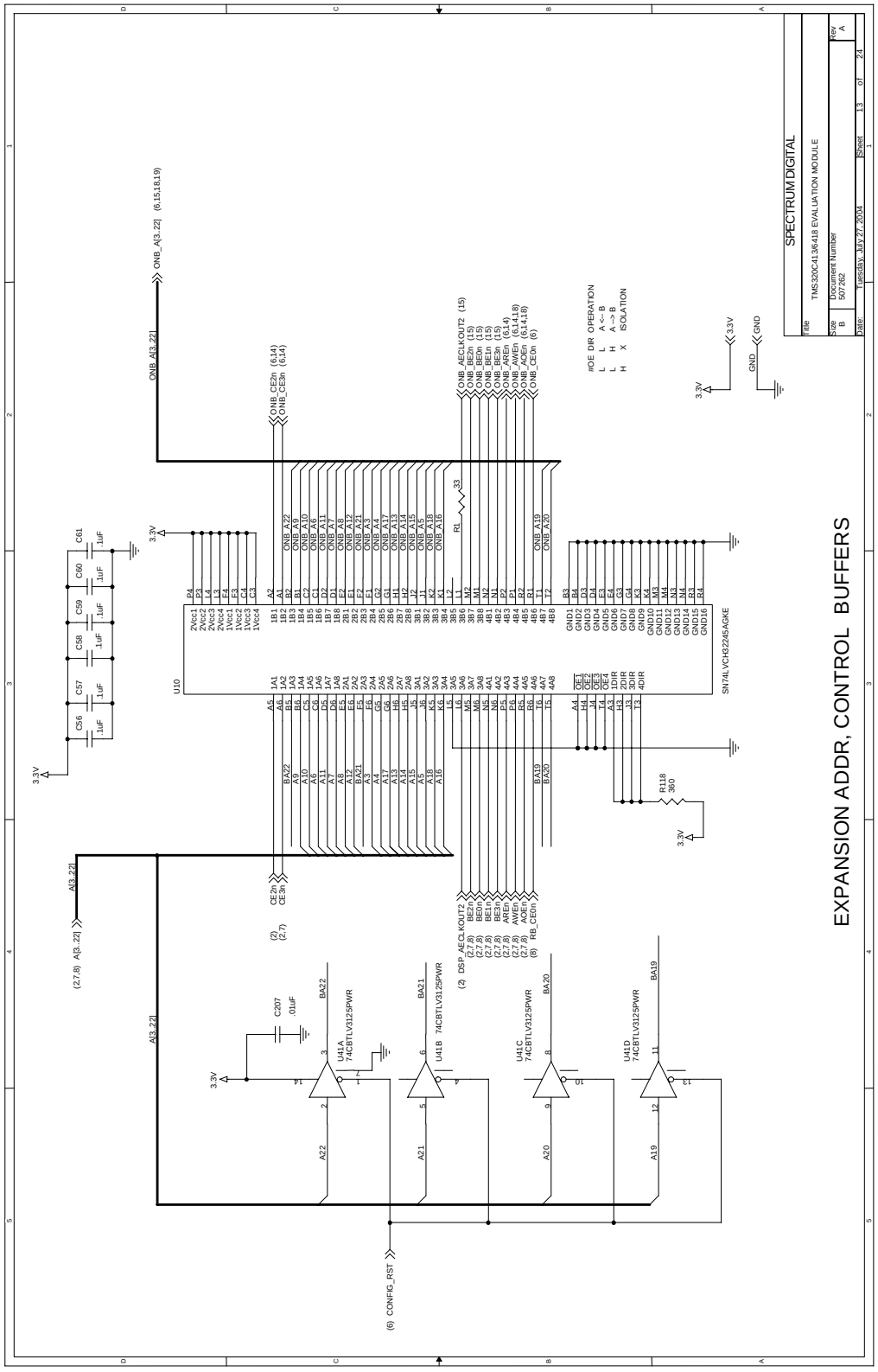

SPECTRUM DIGITAL
Title
TMS320C6418 EVALUATION MODULE
Size
B
Document Number
507262
Rev
A
Date:
Tuesday, July 27, 2004
Sheet
8
of
24
RAMD[0..31] (7,12)
D[0..31] (2)
RN25
RN26
RN27
RN28
RPACK8-33
RAMD0
RAMD1
RAMD2
RAMD3
RAMD4
RAMD5
RAMD6
RAMD7
RAMD8
RAMD9
RAMD10
RAMD11
RAMD12
RAMD13
RAMD14
RAMD15
RAMD16
RAMD17
RAMD18
RAMD19
RAMD20
RAMD21
RAMD22
RAMD23
RAMD24
RAMD25
RAMD26
RAMD27
RAMD28
RAMD29
RAMD30
RAMD31
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
U24
MT48LC2M32B2-MT48LC4M32B2
3.3V
GND
C10 .1uF
C11 .1uF
C12 .1uF
C13 .1uF
R80 10K
R154 10K
R288 0
DSP_CLKMEM
DSP_AECLKOUT1
DSP_SDCKE
SDRAM_CEn
SDWEn
SDCASn
SDRASn
BE0n
BE1n
BE2n
BE3n
RB_CE0n (13)
A[3..22]
(2,7,13) A[3..22]

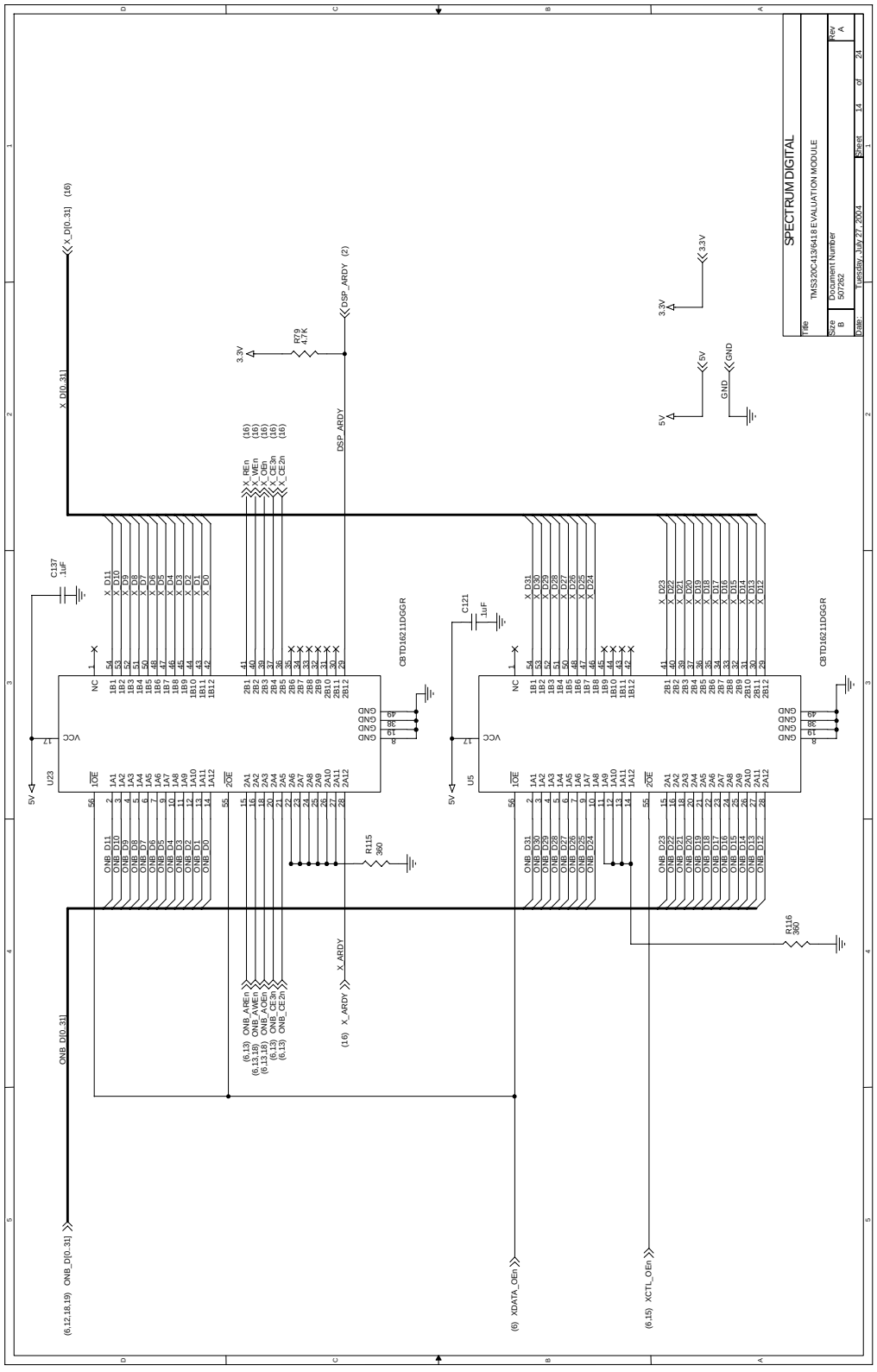

SPECTRUM DIGITAL
TMS320C6413/6418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
I2C EEPROM
HEADER 8X2
24WC256
33 RPACK4
VCC_KEYOARD
3.3V
GND
DSP_SDA0
DSP_SCL0


LEDS/SWITCHES
SPECTRUM DIGITAL
TMS320C6418 EVALUATION MODULE
PWB REVISION IS EMBEDDED IN CPLD REGISTER DIRECTLY
USER LEDS
USER OPTIONS
PUSHBUTTON RESET
3.3V
GND
DSP_RST_LEDn
USER_LED1
USER_LED2
USER_LED3
USER_LED4
PBSW_RSTn
HEADER 8X2
RPACK4-10K
RPACK8-2K
RPACK4-33
SW DIP-4
PUSHBUTTON SW
SN74AHC1G14


SERIAL PORT BUFFER
McBSP0 BUFFER
McBSP1 BUFFER
SPECTRUM DIGITAL
TMS320C41364418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
SN74CBT3245
4.1V
3.3V
GND


EXPANSION DATA BUFFERS
SPECTRUM DIGITAL
TMS320C6418 EVALUATION MODULE
Document Number
507,262
Tuesday, July 27, 2004
ONB_D[0..31] (6,14,18,19)
ONB_D[0..31]
RAMD[0..31]
(7,8) RAMD[0..31]
(6) ONB_XDATA_T/Rn
(6) ONB_XDATA_OEn
3.3V
GND
U8
SN74LVCH32245AGKE
#OE DIR OPERATION
L L A <- B
L H A -> B
H X ISOLATION
C52 1uF
C53 1uF
C54 1uF
C55 1uF
C48 1uF
C49 1uF


EXPANSION ADDR, CONTROL BUFFERS
SPECTRUM DIGITAL
TMS320C41364418 EVALUATION MODULE
Document Number
507262
Rev A
Sheet 13 of 24
Tuesday, July 27, 2004
ONB_A[3..22] (6,15,18,19)
A[3..22]
(2,7,8) A[3..22]
(6) CONFIG_RST
ONB_CE2n (6,14)
ONB_CE3n (6,14)
(2) CE2n
(2,7) CE3n
ONB_AECLKOUT2 (15)
ONB_BE2n (15)
ONB_BE0n (15)
ONB_BE1n (15)
ONB_BE3n (15)
ONB_AOEn (6,14,18)
ONB_AWEn (6,14,18)
ONB_CE0n (6)
(2) DSP_AECLKOUT2
(2,7,8) BE2n
(2,7,8) BE0n
(2,7,8) BE1n
(2,7,8) BE3n
(2,7,8) AOEn
(2,7,8) AWEn
(8) RB_CE0n
ONB_A22
ONB_A9
ONB_A10
ONB_A11
ONB_A7
ONB_A8
ONB_A23
ONB_A21
ONB_A3
ONB_A4
ONB_A17
ONB_A13
ONB_A14
ONB_A15
ONB_A5
ONB_A18
ONB_A16
ONB_A19
ONB_A20
#OE DIR OPERATION
L L A <- B
L H A -> B
H X ISOLATION
U10
SN74LVCH32245AGKE
U41A 74CBTLV3125PWR
U41B 74CBTLV3125PWR
U41C 74CBTLV3125PWR
U41D 74CBTLV3125PWR
BA22
BA21
BA20
BA19
A22
A21
A20
A19
C207 .01uF
C56 .1uF
C57 .1uF
C58 .1uF
C59 .1uF
C60 .1uF
C61 .1uF
R118 360
RL 33
3.3V
GND


SPECTRUM DIGITAL
Title
TMS320C6413/6418 EVALUATION MODULE
Size
B
Document Number
507262
Rev
A
Date:
Tuesday, July 27, 2004
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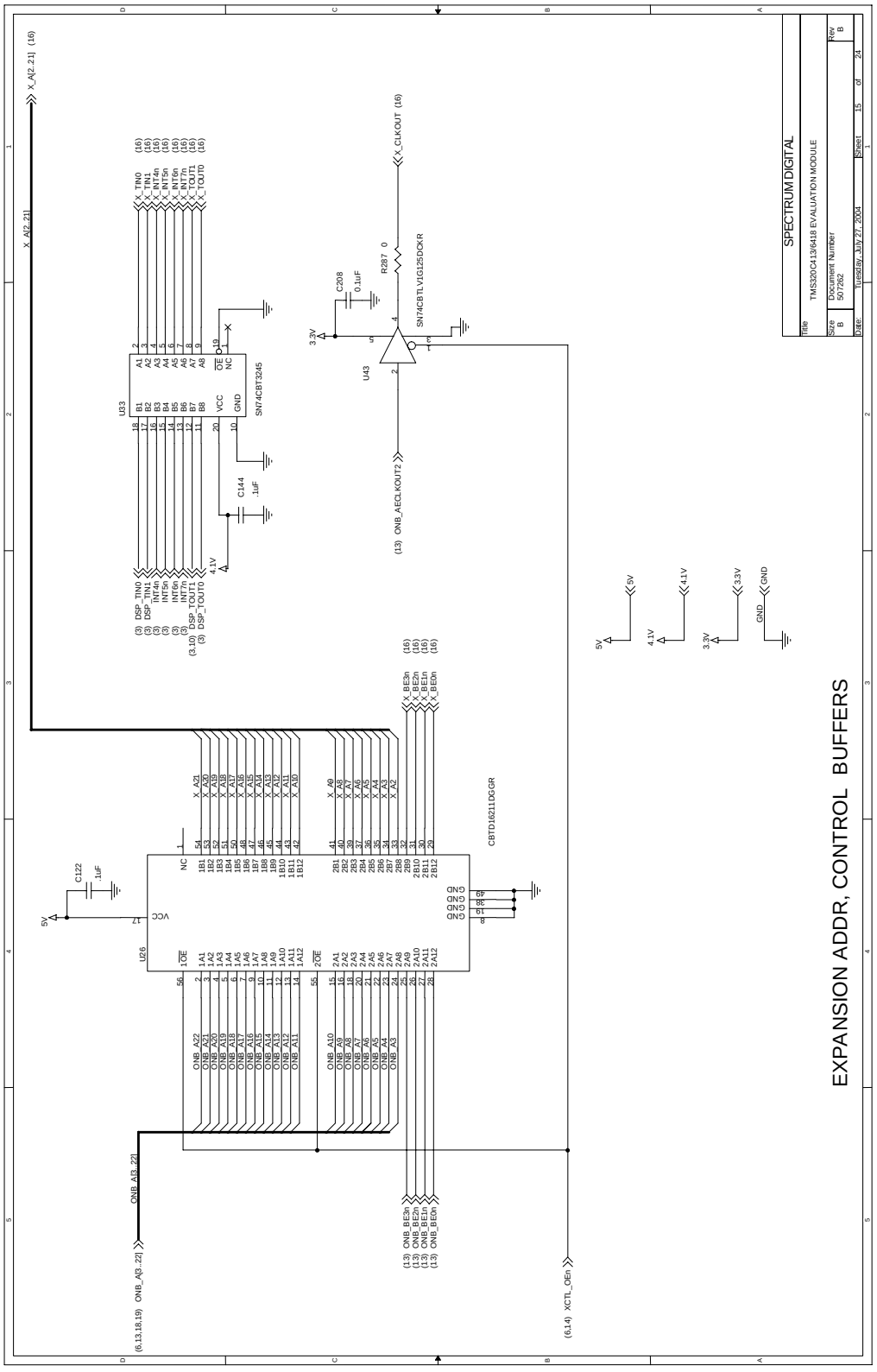
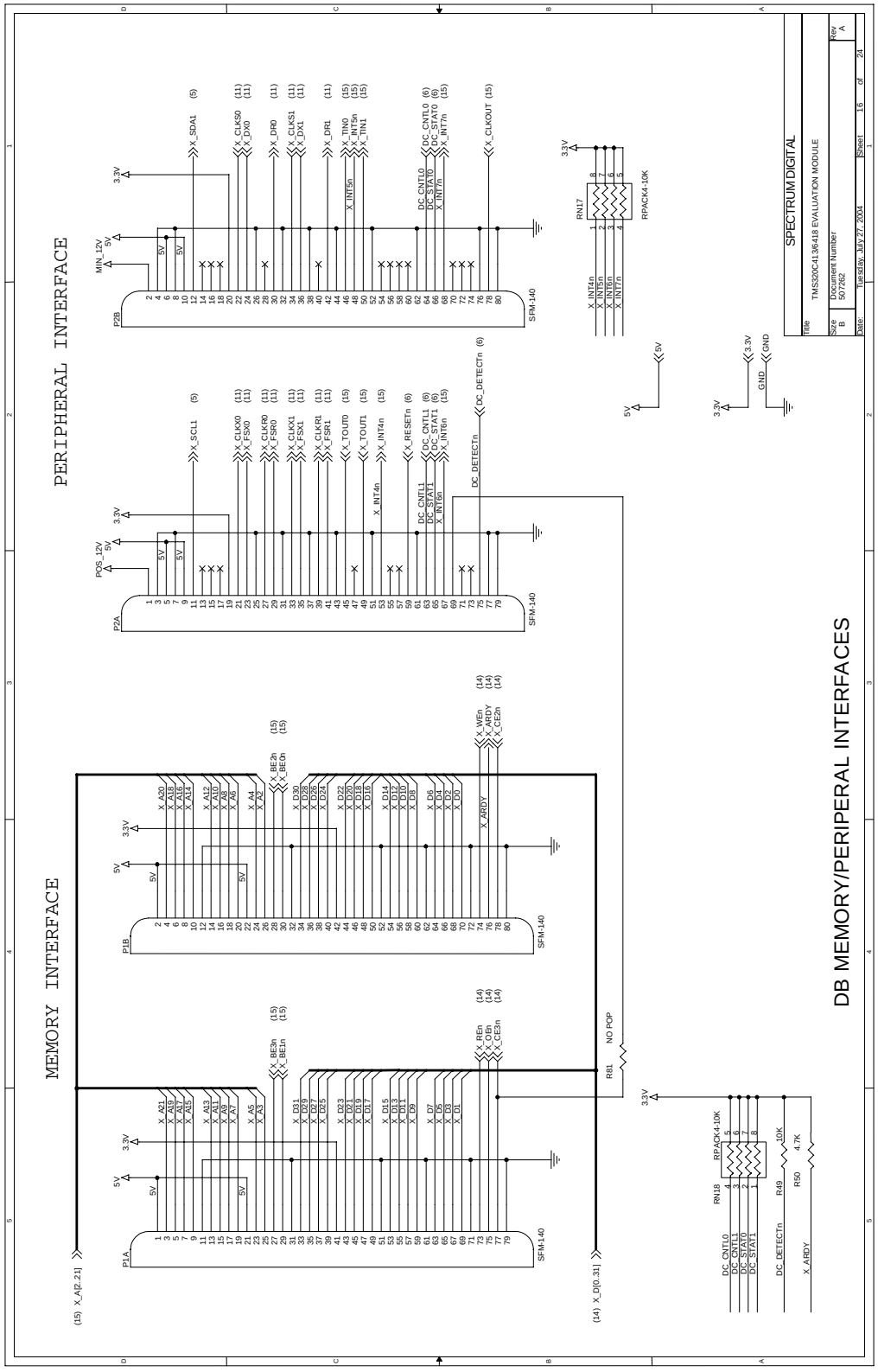
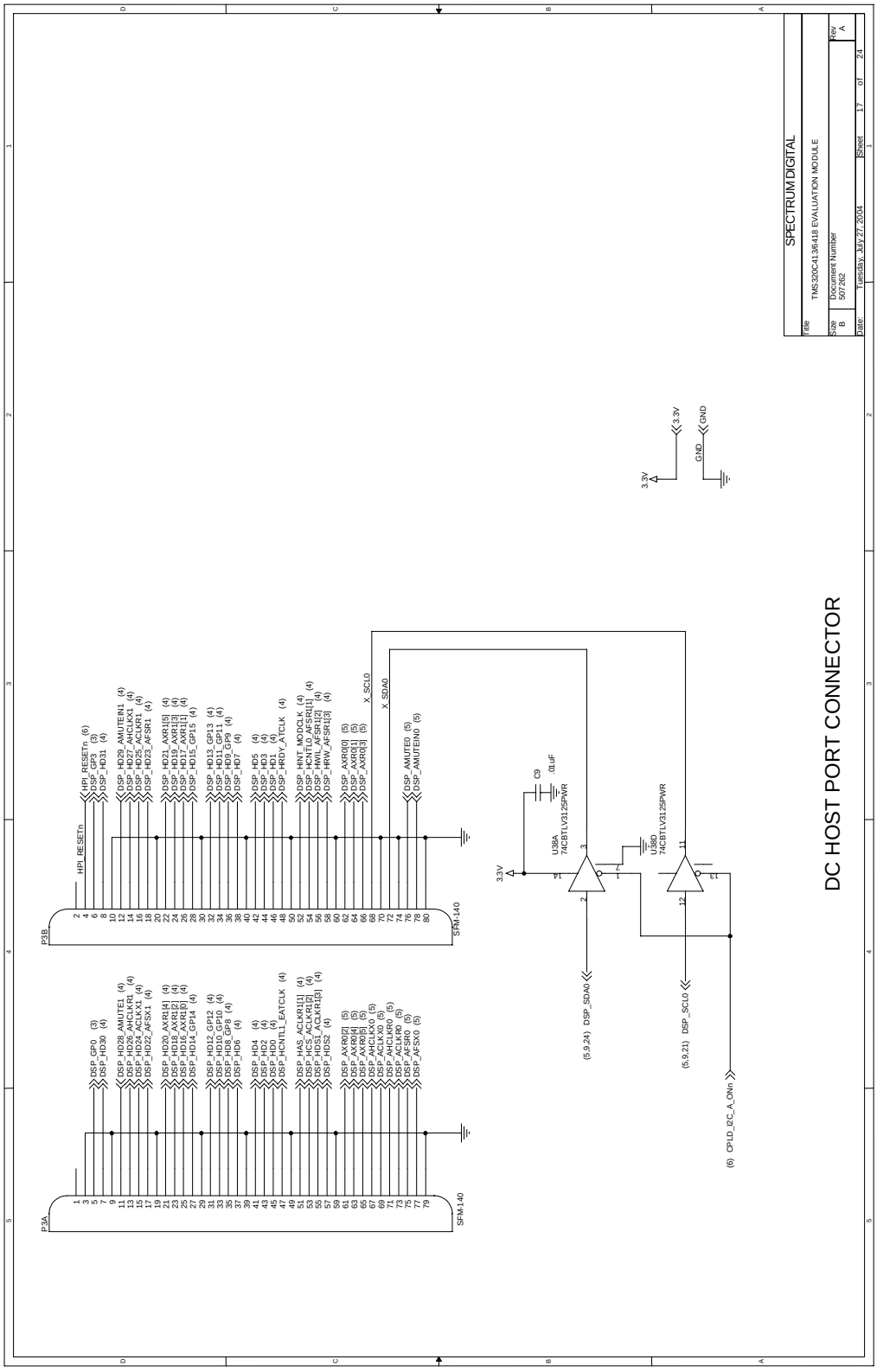
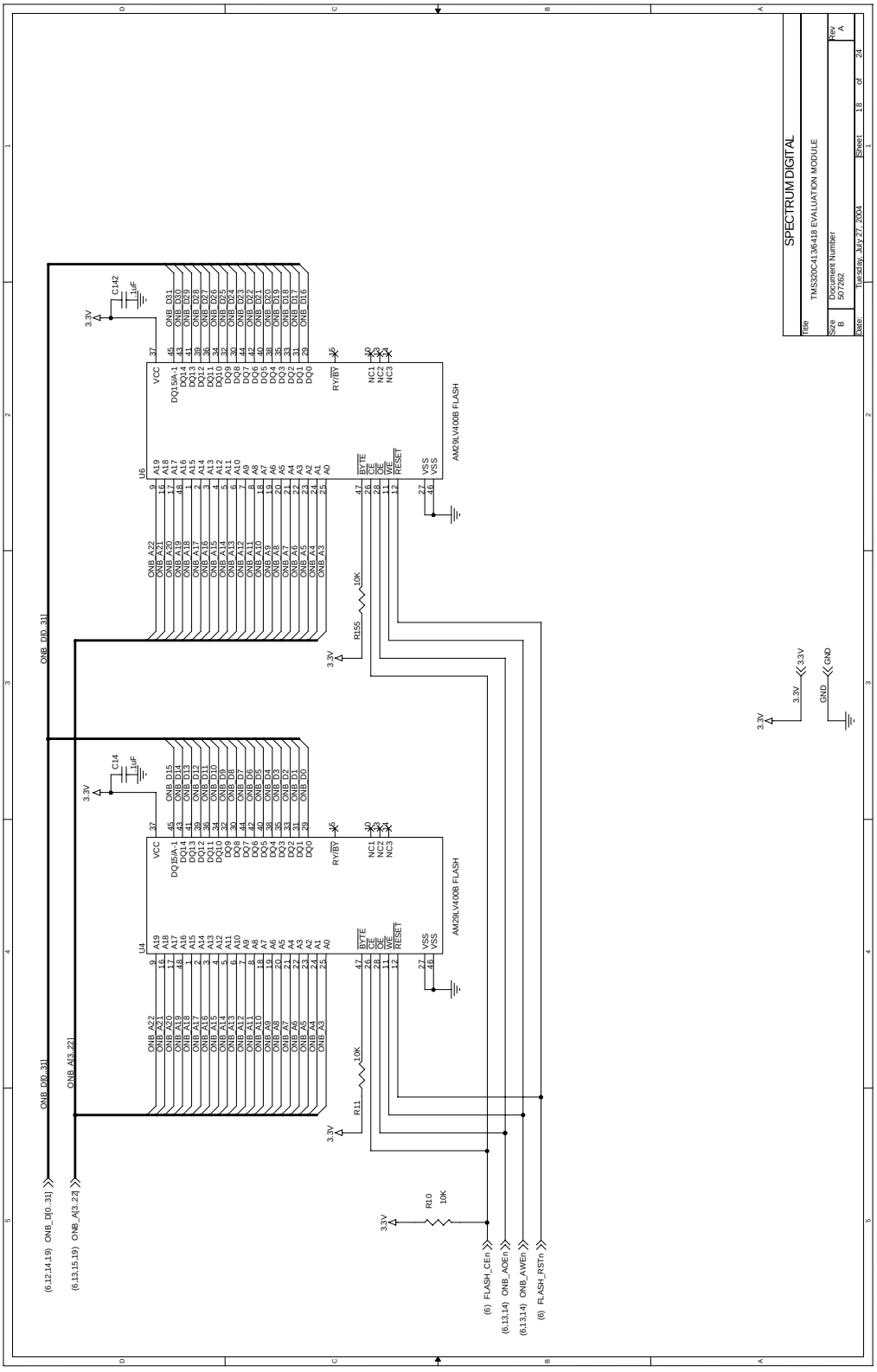
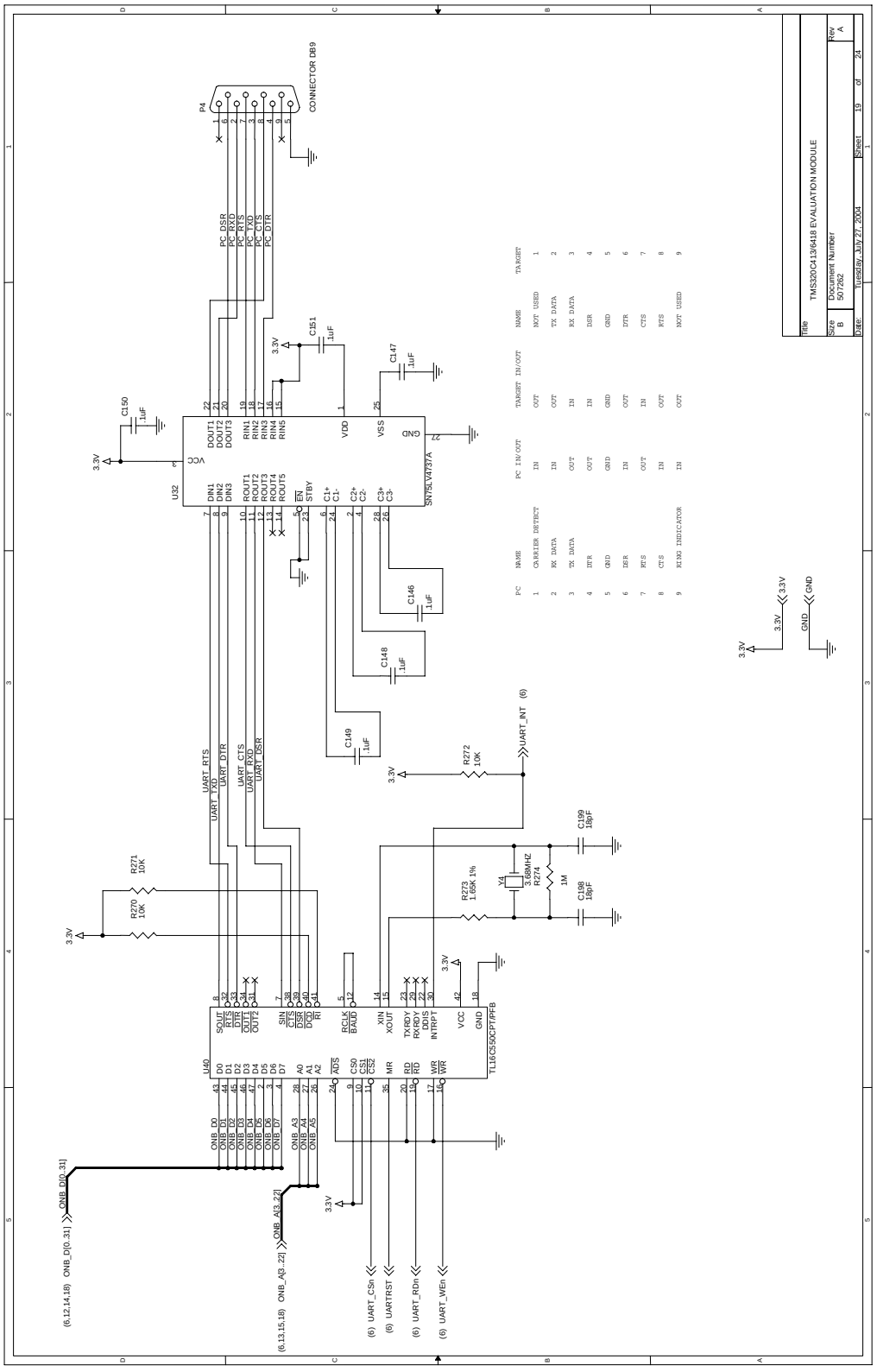
14
of
24
X_D[0..31]
DSP_ARDY
X_REn
X_WEn
X_CE3n
X_CE2n
X_ARDY
ONB_D[0..31]
U23
U5
CBTD16211DGGR
C137
.1uF
C121
.1uF
R79
4.7K
R115
360
R116
360
3.3V
5V
GND
(6.12,18,19) ONB_D[0..31]
(6) XDATA_OEn
(6,15) XCTL_OEn

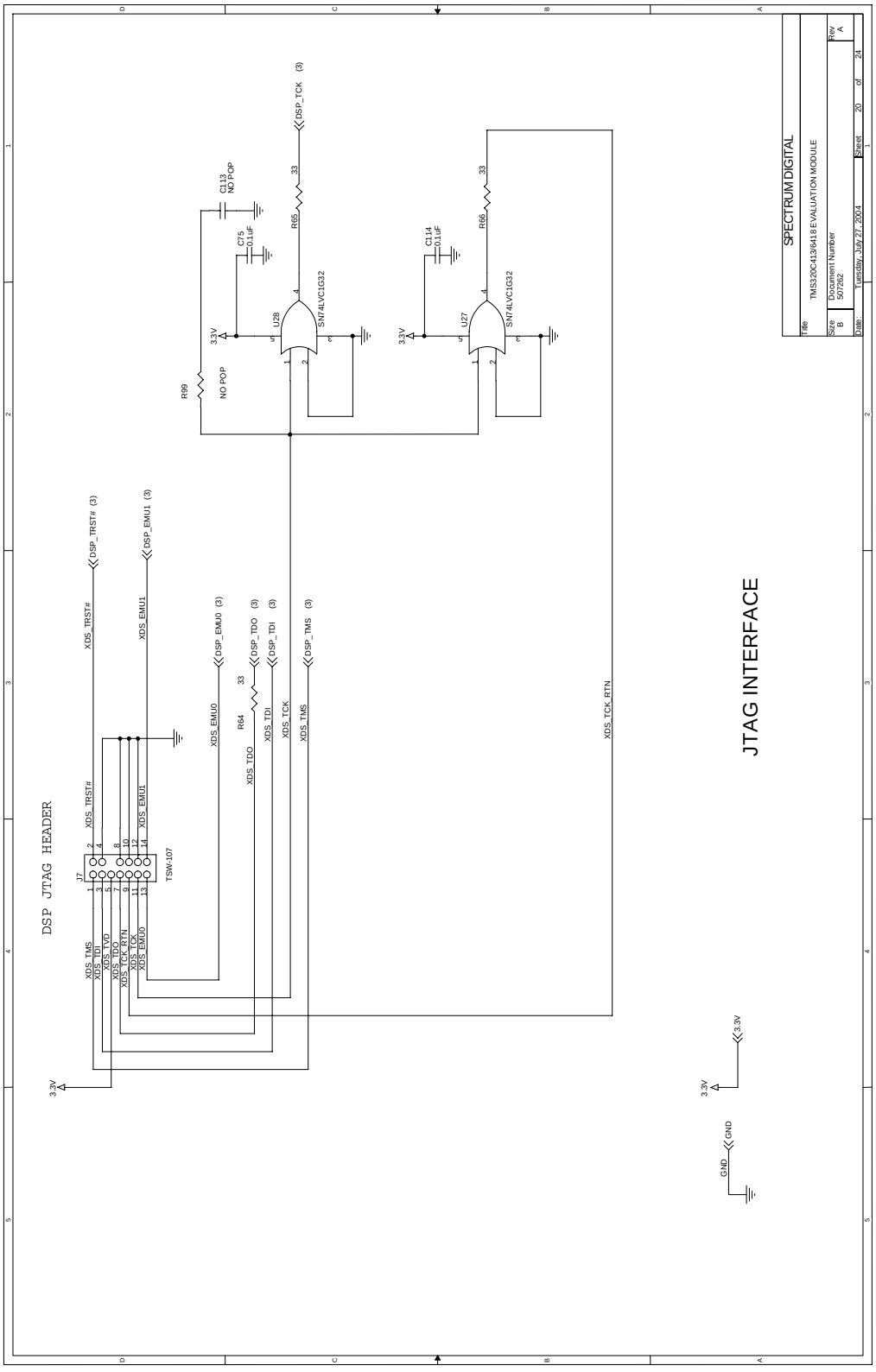

EXPANSION ADDR, CONTROL BUFFERS
SPECTRUM DIGITAL
TMS320C413/6418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
SN74CBT3245
SN74CBTLV1G125DCKR
CBTD16211DGGR
C122 .1uF
C144 .1uF
C208 0.1uF
R287 0
U19
U33
U43
U26
X_A[2..21]
ONB_A[3..22]
X_CLKOUT
ONB_AECLKOUT2
XCTL_OEn
5V
4.1V
3.3V
GND


DB MEMORY/PERIPERAL INTERFACES
MEMORY INTERFACE
PERIPHERAL INTERFACE
SPECTRUM DIGITAL
TMS320C41/36-419 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
NO POP
R81
R49
10K
R50
4.7K
RPACK4-10K
SFM-140


DC HOST PORT CONNECTOR
SPECTRUM DIGITAL
TMS320C41364418 EVALUATION MODULE
Document Number
507-282
Tuesday, July 27, 2004
Sheet 17 of 24
Rev A
P3A
SFM-140
P3B
SFM-140
HPI_RESETn
3.3V
GND
U38A
74CBTLV3125PWR
U38D
74CBTLV3125PWR
C9
.01uF
X_SCL0
X_SDA0
(5,9,24) DSP_SDA0
(5,9,21) DSP_SCL0
(6) CPLD_I2C_A_ONn


SPECTRUM DIGITAL
TMS320C41/36419 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
AM29LV400B FLASH
ONB_D[0..31]
ONB_A[3..22]
(6,12,14,19) ONB_D[0..31]
(6,13,15,19) ONB_A[3..22]
(6) FLASH_CEn
(6,13,14) ONB_AOEn
(6,13,14) ONB_AWEn
(6) FLASH_RSTn
3.3V
GND
R10 10K
R11 10K
R155 10K
C14 1uF
C142 1uF


TMS320C413/6418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
CONNECTOR DB9
SN75LV4737A
TL16C550CPTPFB
UART_INT (6)
3.68MHZ
1.65K 1%
1M
10K
10uF
.1uF
1uF
3.3V
GND


JTAG INTERFACE
DSP JTAG HEADER
J7
TSW-107
XDS_TMS
XDS_TDI
XDS_TVD
XDS_TDO
XDS_TCK_RTN
XDS_TCK
XDS_EMU0
XDS_TRST#
XDS_EMU1
DSP_TRST# (3)
DSP_EMU1 (3)
DSP_EMU0 (3)
DSP_TDO (3)
DSP_TDI (3)
DSP_TMS (3)
DSP_TCK (3)
R64
33
R65
33
R66
33
R99
NO POP
C113
NO POP
C75
0.1uF
C114
0.1uF
U28
U27
SN74LVC1G32
3.3V
GND
SPECTRUM DIGITAL
TMS320C6418 EVALUATION MODULE
Document Number
507362
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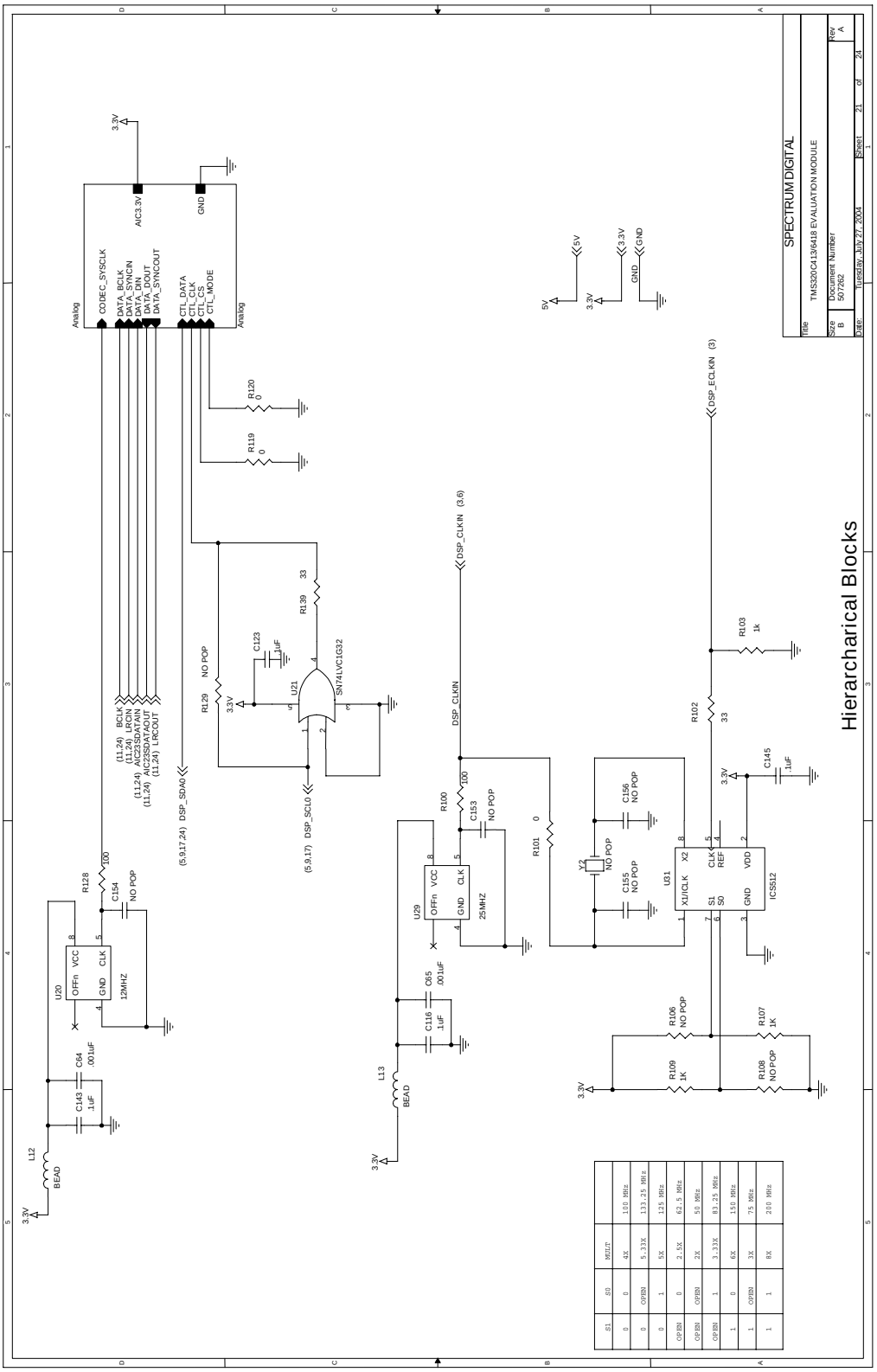
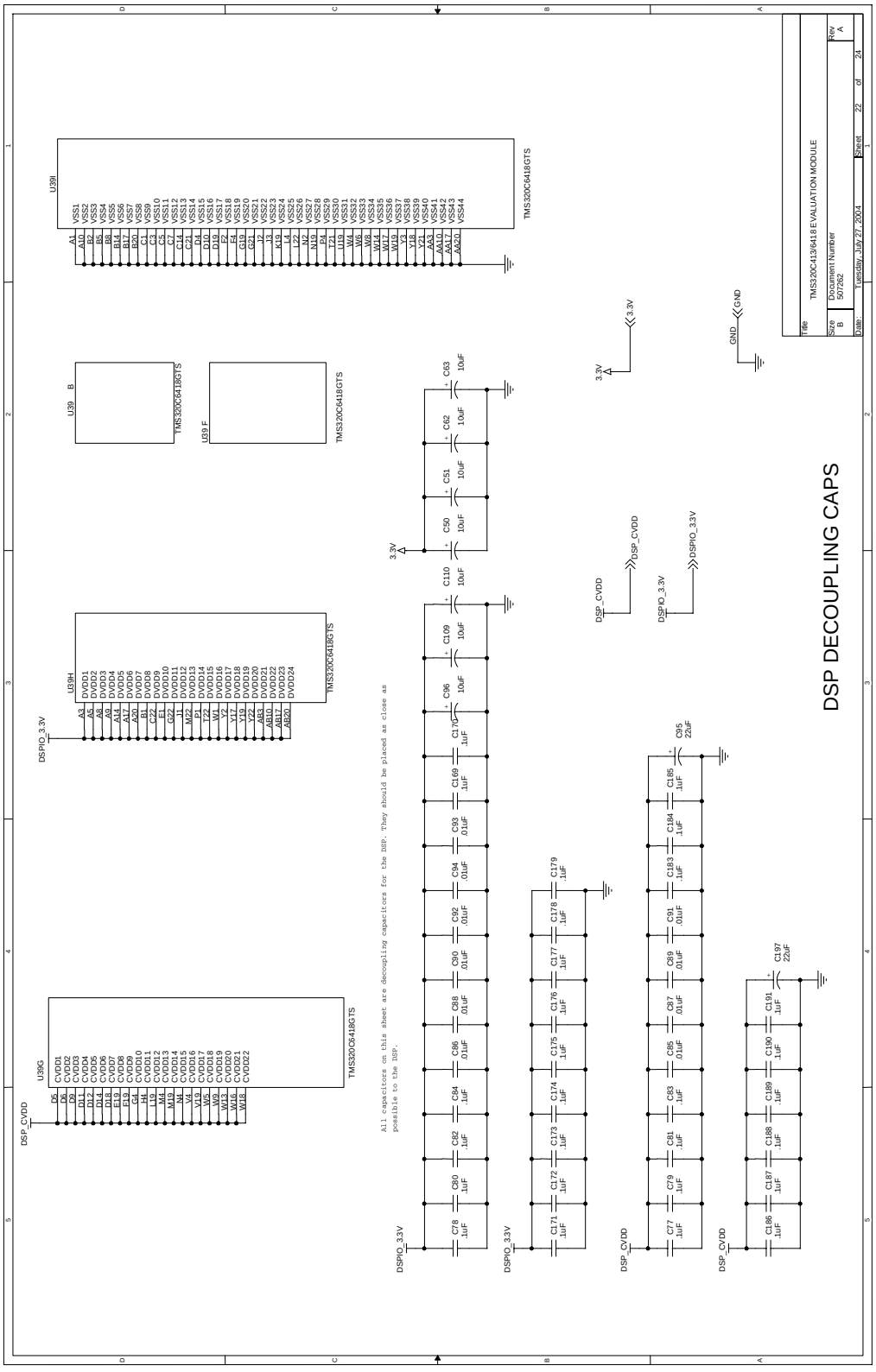
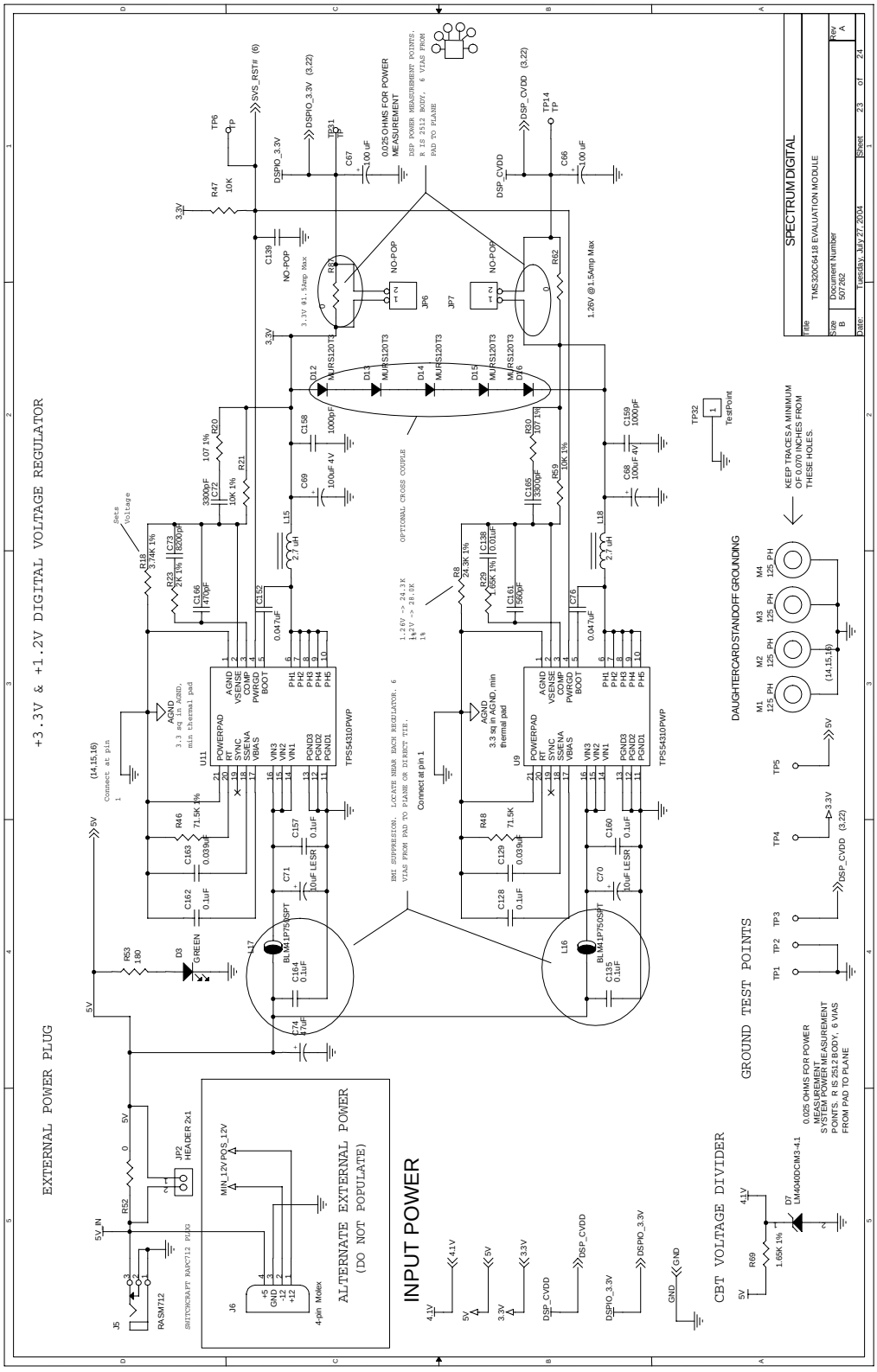
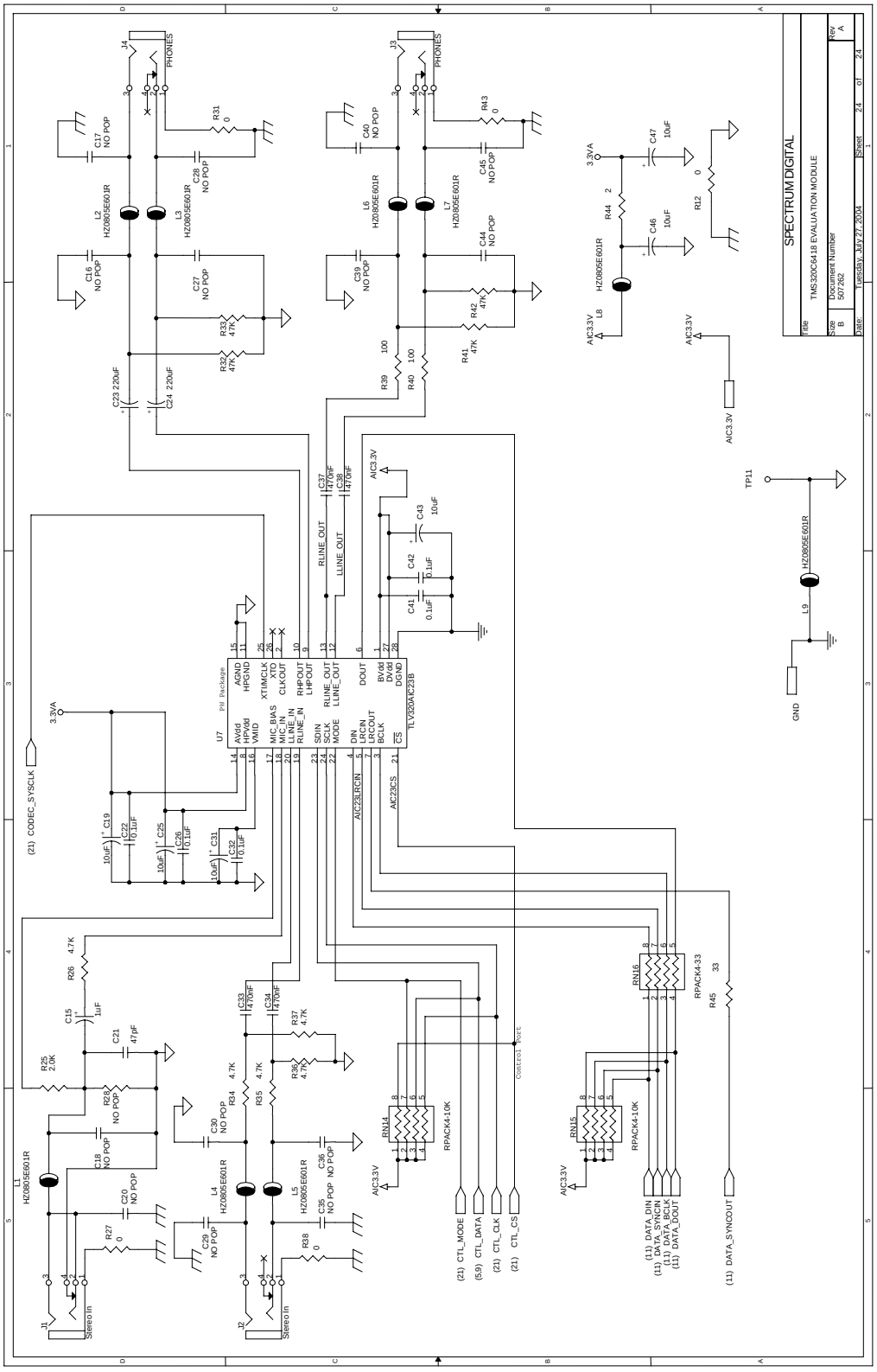
Rev A


Hierarchical Blocks
SPECTRUM DIGITAL
TMS320C6413/6418 EVALUATION MODULE
Document Number
507262
Tuesday, July 27, 2004
CODEC_SYSCLK
DATA_BCLK
DATA_WCLK
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
CTL_DATA
CTL_CLK
CTL_CS
CTL_MODE
AIC3.3V
GND
DSP_CLKIN
DSP_SDA0
DSP_SCL0
DSP_ECLKIN
SN74LVC1G32
ICS512
12MHZ
25MHZ
BEAD


DSP DECOUPLING CAPS
TMS320C6418 EVALUATION MODULE
Document Number
507362
Tuesday, July 27, 2004
Sheet 22 of 24
All capacitors on this sheet are decoupling capacitors for the DSP. They should be placed as close as possible to the DSP.
TMS320C6418GTS
DSP_CVDD
DSPIO_3.3V
3.3V
GND


+3.3V & +1.2V DIGITAL VOLTAGE REGULATOR
EXTERNAL POWER PLUG
INPUT POWER
ALTERNATE EXTERNAL POWER
(DO NOT POPULATE)
GROUND TEST POINTS
CBT VOLTAGE DIVIDER
DAUGHTERCARDSTANDOFF GROUNDING
SPECTRUM DIGITAL
TMS320C6418 EVALUATION MODULE
TPS54310PWP
RASM712
MIN_12V POS_12V
4-pin Molex
0.025 OHMS FOR POWER MEASUREMENT
KEEP TRACES A MINIMUM OF 0.070 INCHES FROM THESE HOLES.
1.26V @1.5Amp Max
3.3V @1.5Amp Max
OPTIONAL CROSS COUPLE
EMI SUPPRESION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.
1.26V -> 24.3K
1.2V -> 28.0K
1%
Connect at pin 1
Sets Voltage
3.3 mA to AGND, min thermal pad
Tuesday, July 27, 2004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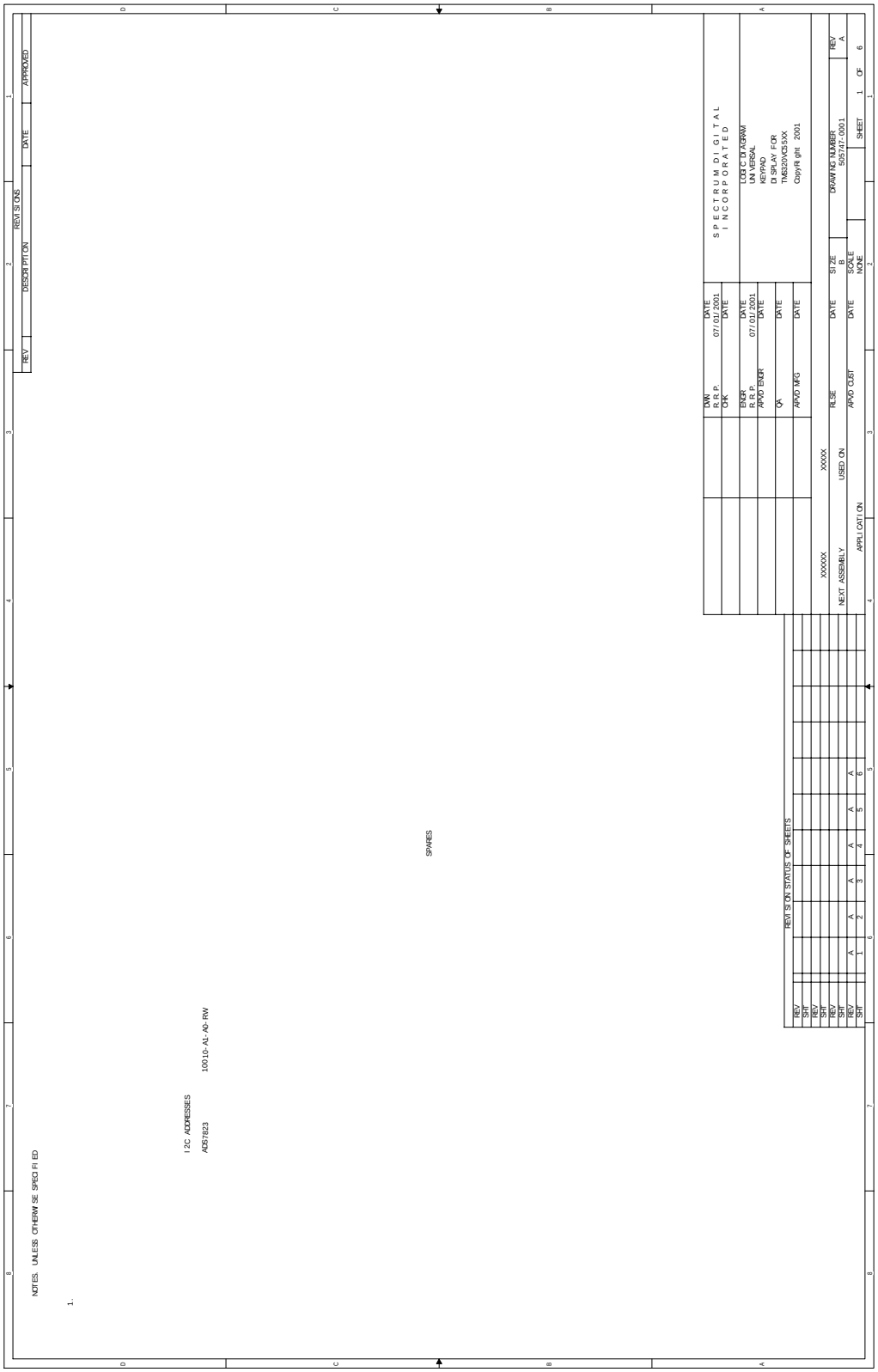
TMS320C6418 EVALUATION MODULE
Document Number
507.262
Tuesday, July 27, 2004
Sheet 24 of 24
Rev A
TLV320AIC23B
Stereo In
PHONES
Control Port
(21) CODEC_SYSCLK
(21) CTL_MODE
(5,9) CTL_DATA
(21) CTL_CLK
(21) CTL_CS
(11) DATA_SYNCIN
(11) DATA_BCLK
(11) DATA_DOUT
(11) DATA_SYNCOUT
AIC3.3V
3.3VA
GND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REV
DESCRIPTION
DATE
APPROVED
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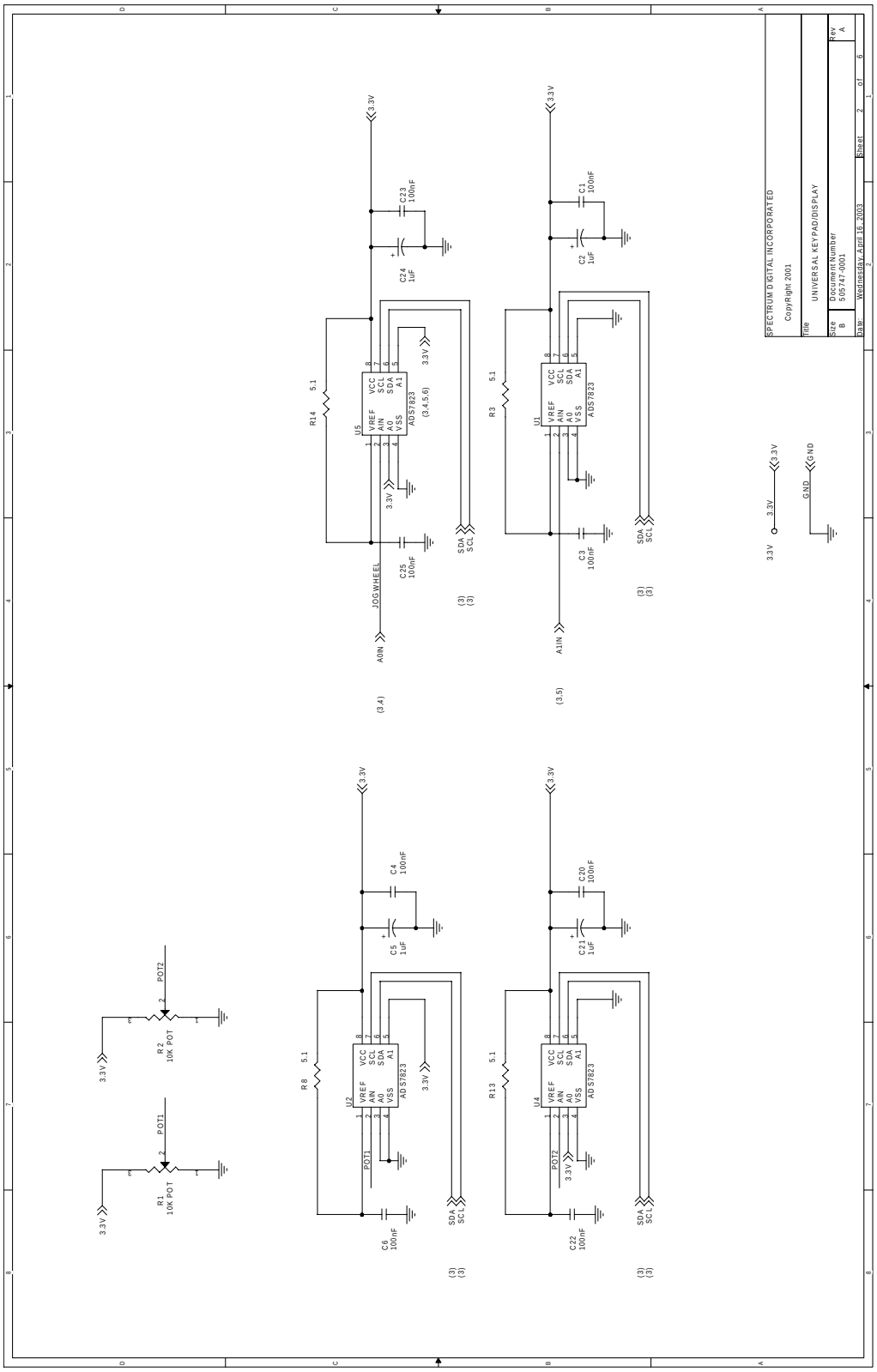
1.
I2C ADDRESSES
ADS7823
1001b-A1-A0-RW
SPARES
REVISION STATUS OF SHEETS
SPECTRUM DIGITAL
INCORPORATED
DRAWN
R.R.P.
07/01/2001
CHK
ENGR
R.R.P.
07/01/2001
APVD ENGR
QA
APVD MFG
DATE
XXXXX
XXXXX
NEXT ASSEMBLY
USED ON
APPLICATION
REL'SE
APVD CUST
SIZE
B
SCALE
NONE
DRAWING NUMBER
505747-0001
REV
A
SHEET 1 OF 6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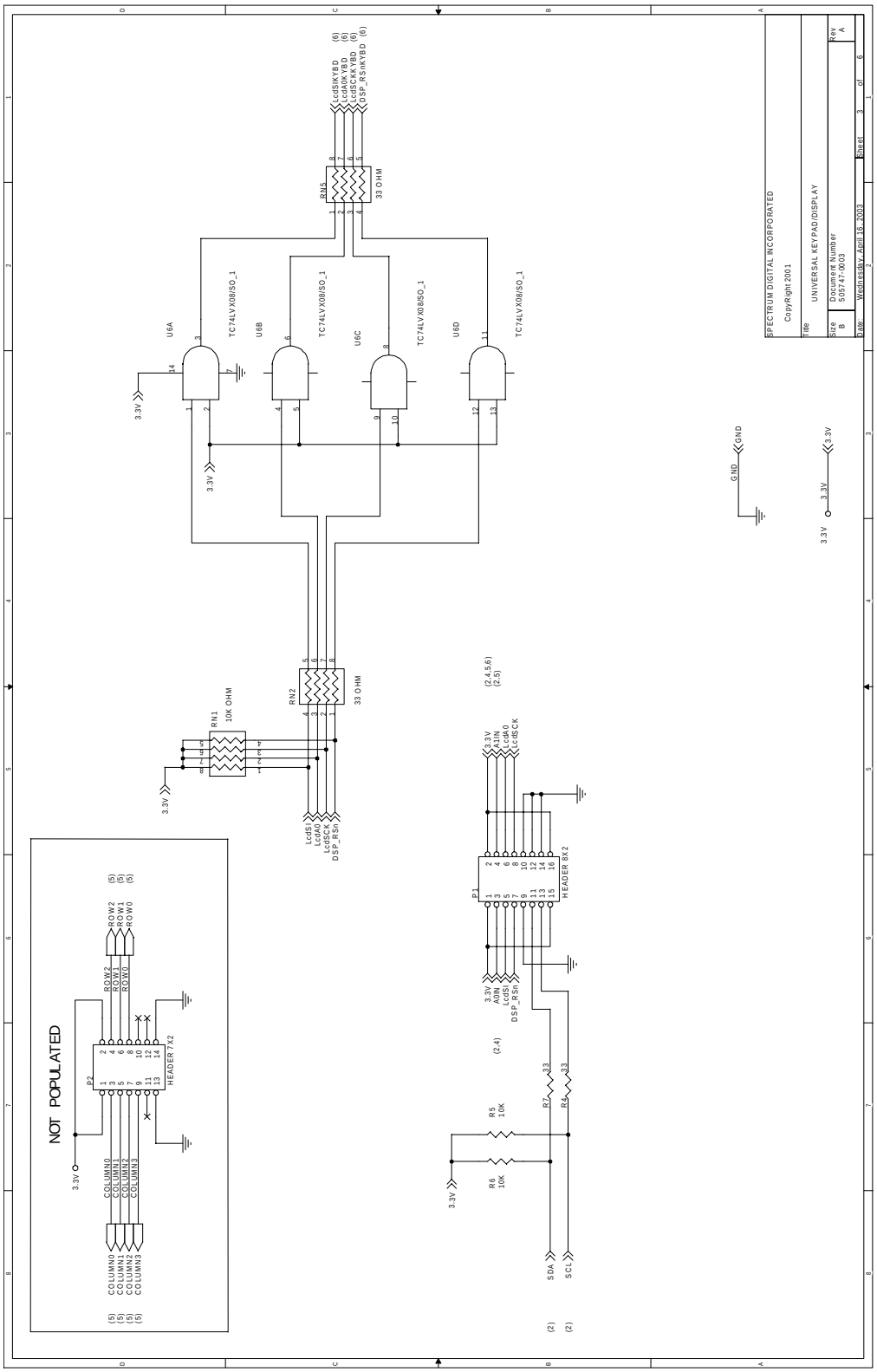
UNIVERSAL KEYPAD/DISPLAY
Size B
Document Number 505747-0001
Rev A
Date: Wednesday, April 16, 2003
Sheet 2 of 6
U5
U1
U2
U4
ADS7823
VCC SCL SDA A1
VREF AIN A0 VSS
R14 5.1
R3 5.1
R8 5.1
R13 5.1
C23 100nF
C24 1uF
C1 100nF
C2 1uF
C4 100nF
C5 1uF
C20 100nF
C21 1uF
C25 100nF
C3 100nF
C6 100nF
C22 100nF
3.3V
GND
JOGWHEEL
AIIN
AIOUT
POT1
POT2
R1 10K POT
R2 10K POT
SDA
SCL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Rev
A
Date:
Wednesday, April 16, 2003
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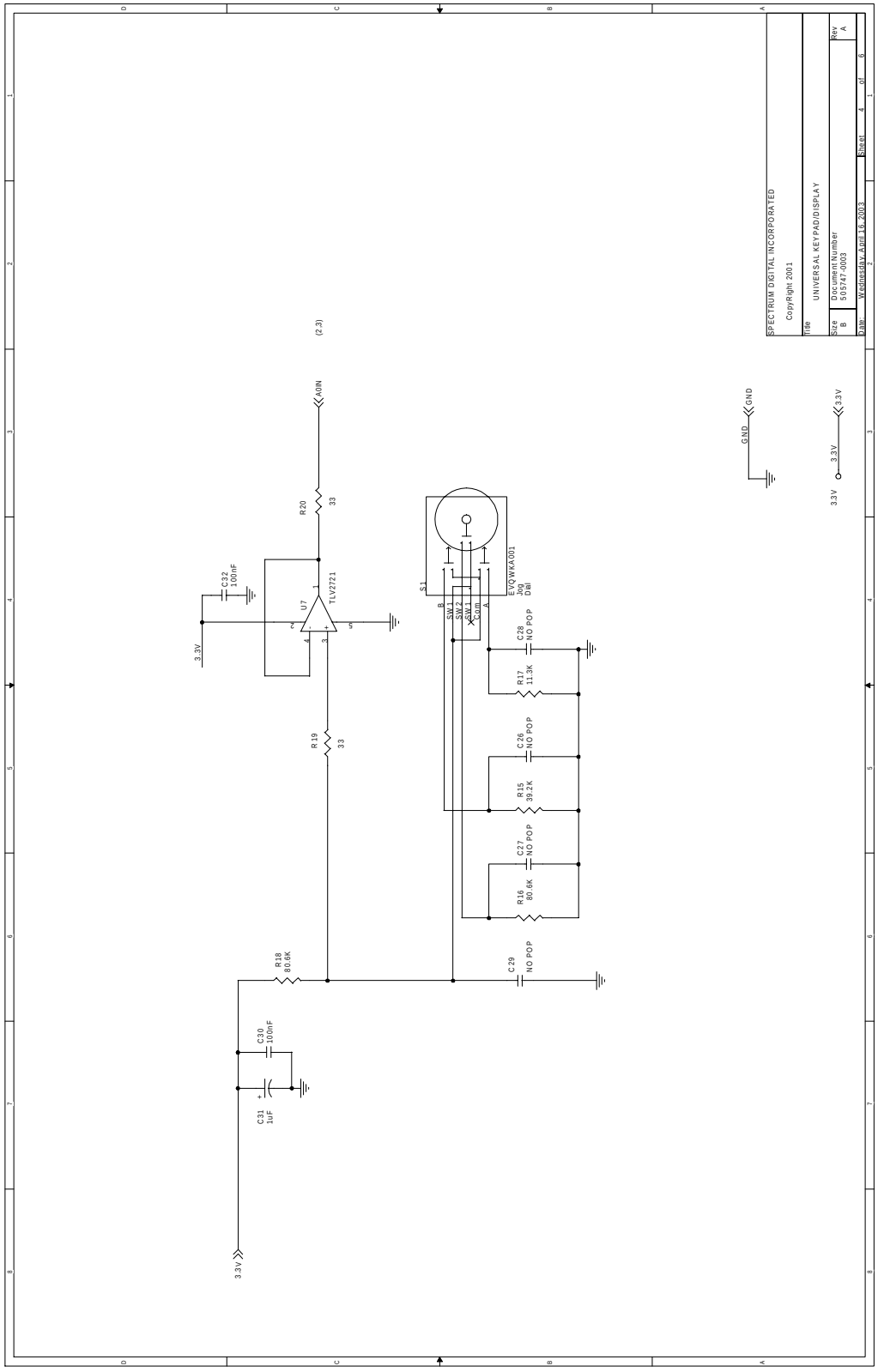
3
of
6
U6A
U6B
U6C
U6D
TC74LVX08/SO_1
RN5
33 OHM
RN2
33 OHM
RN1
10K OHM
P1
HEADER 8X2
P2
HEADER 7X2
NOT POPULATED
R5
10K
R6
10K
R7
33
R4
33
3.3V
GND
SDA
SCL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505747-0003
Rev
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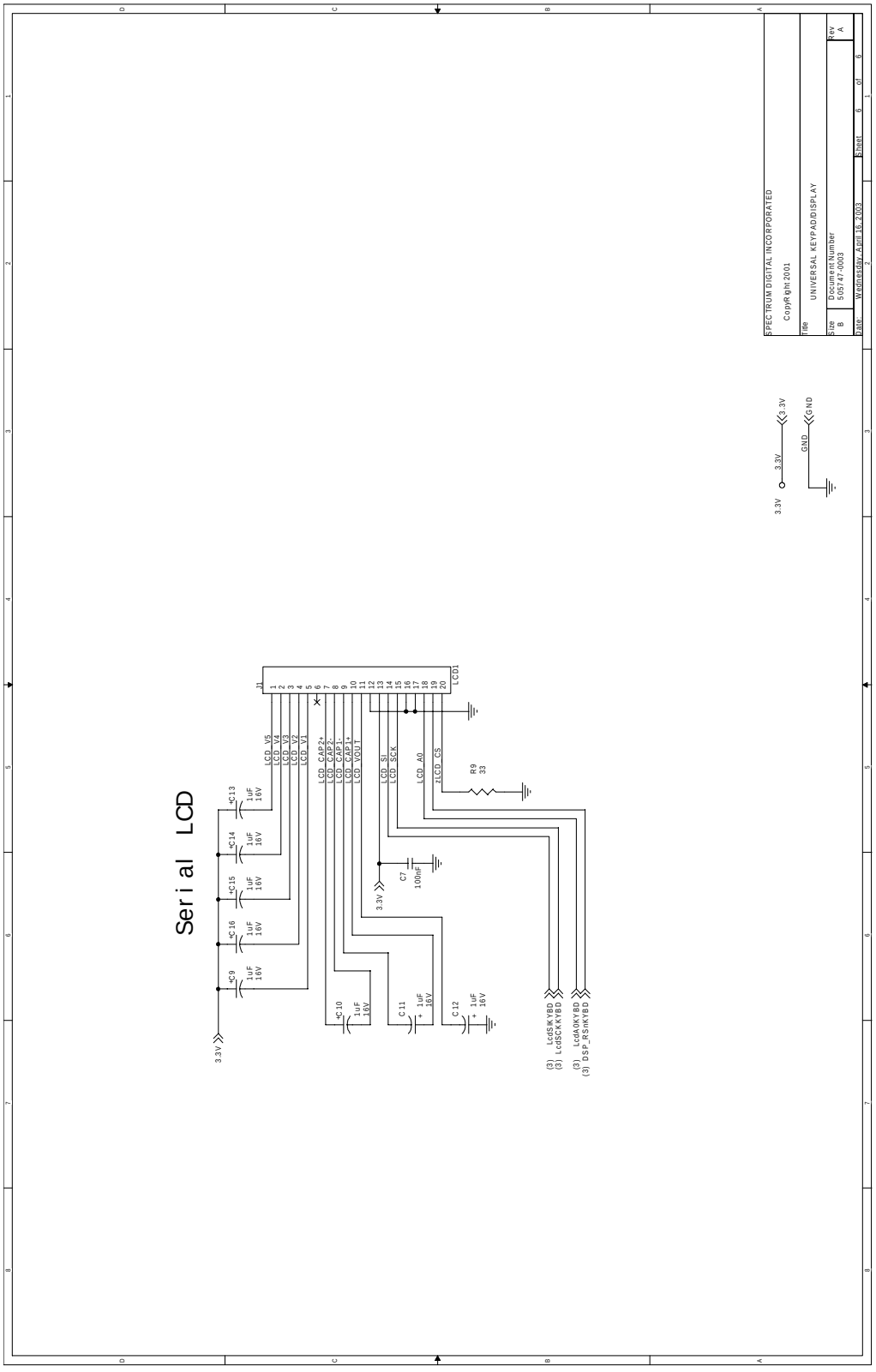
Sheet
4
of
6
(2.3)
+10V
R20
33
C32
100nF
U7
TLV2721
3.3V
R19
33
S1
EVQWK4001
Jog
Dial
B
SW1
SW2
SW1
Com
A
C28
NO POP
R17
11.3K
C26
NO POP
R15
39.2K
C27
NO POP
R16
80.6K
R18
80.6K
C29
NO POP
C30
100nF
C31
1uF
3.3V
GND
3.3V
3.3V


Serial LCD
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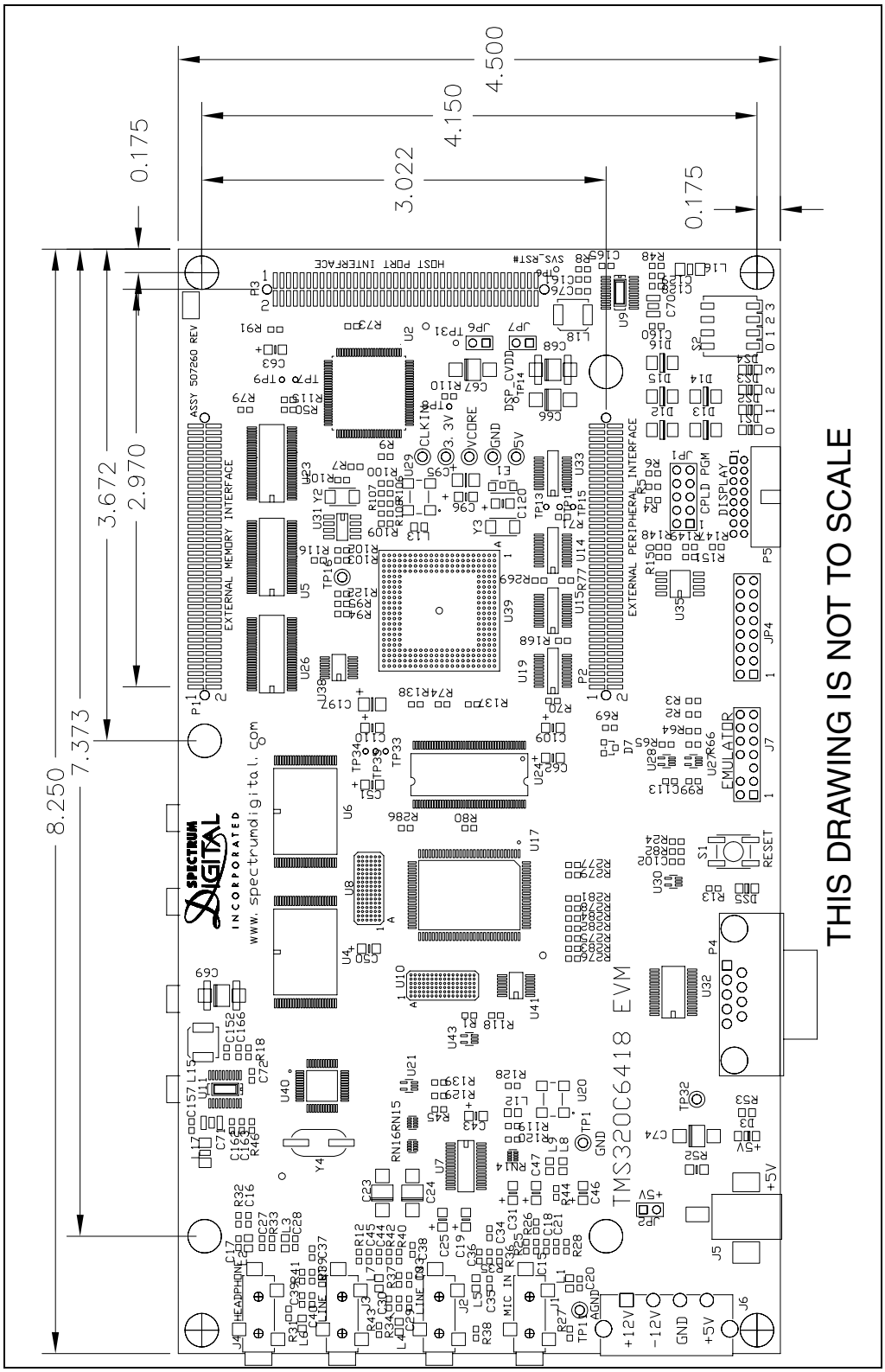
Wednesday, April 16, 2003
Sheet
6
of
6
3.3V
GND
J1
LCD1
LCD_V5
LCD_V4
LCD_V3
LCD_V2
LCD_V1
LCD_CAP2+
LCD_CAP2-
LCD_CAP1-
LCD_CAP1+
LCD_VOUT
LCD_SI
LCD_SCK
LCD_A0
zLCD_CS
R9
33
C7
100nF
C9
C10
C11
C12
C13
C14
C15
C16
1uF
16V
(3) LcdSCKVBD
(3) LcdSCKVBD
(3) LcdAOKVBD
(3) DSP_RSiMKTBD

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320C6413/C6418 EVM and Keypad/display Module produced by Spectrum Digital.

Topic **Page**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8.250
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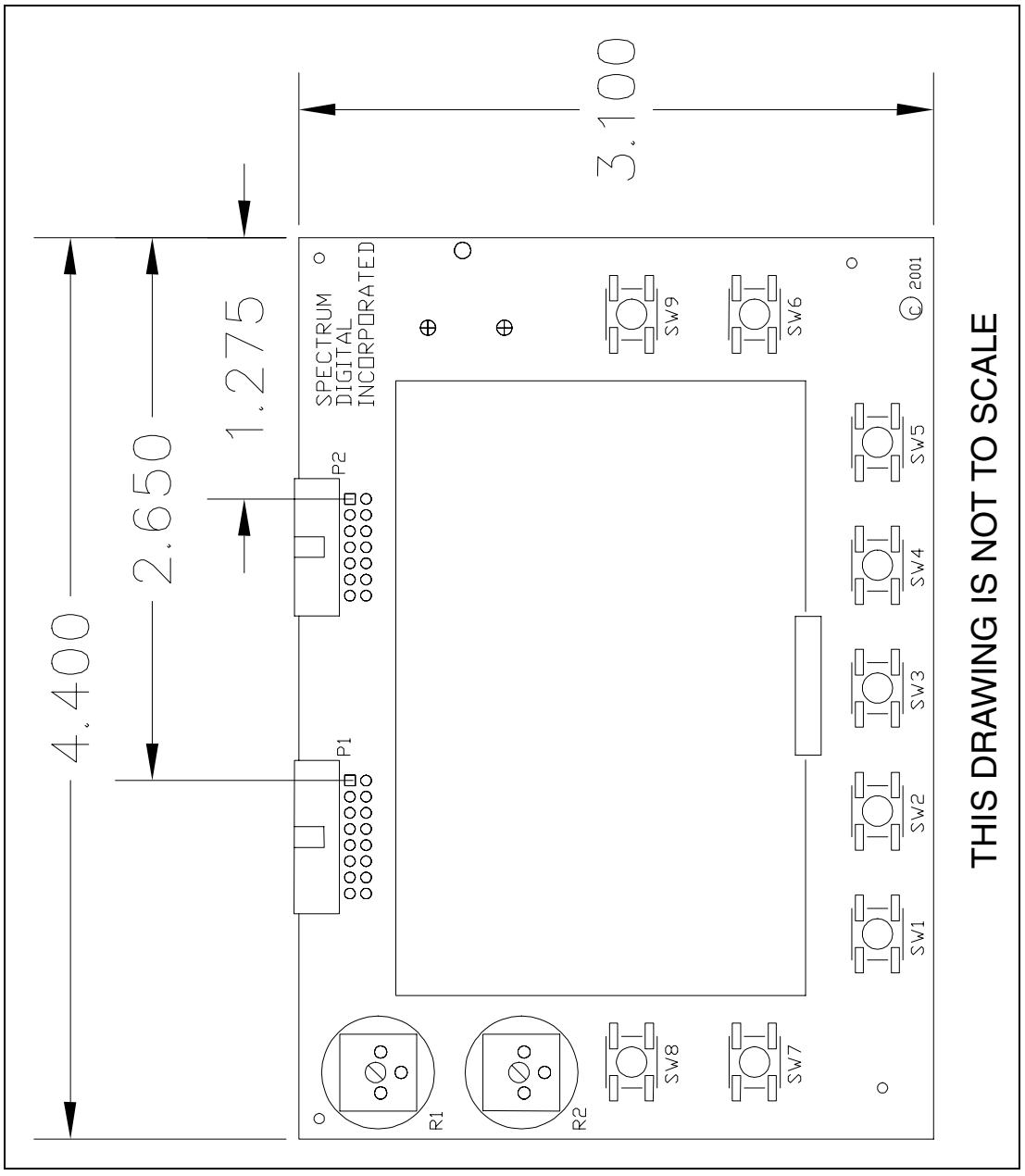
TMS320C6418 EVM
www.spectrumdigital.com
SPECTRUM DIGITAL INCORPORATED
HOST PORT INTERFACE
EXTERNAL MEMORY INTERFACE
EXTERNAL PERIPHERAL INTERFACE
HEADPHONE
MIC IN
LINE IN
EMULATOR
RESET
DISPLAY
CPLD PGM
+12V
-12V
GND
+5V


3.100
4.400
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1.275
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P1
P2
R1
R2
SW1
SW2
SW3
SW4
SW5
SW6
SW7
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