SPECTRUM DIGITAL
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SPI515 Adjustable Voltage Parallel Port JTAG Emulator

Installation
Guide

1999   *DSP Development Systems*

SPI515 Adjustable
Voltage Parallel Port
JTAG Emulator
Installation Guide

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Contents

About This Manual

This document describes the module level operations of the SPI515 Adjustable Voltage Parallel Port JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator will sometimes be referred to as the SPI515.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer Users Guide
Texas Instruments High Level Language Debugger Users Guide

Chapter 1

Introduction to the SPI515 Adjustable Voltage Parallel Port JTAG Emulator

This chapter provides you with a description of the SPI515 Adjustable Voltage Parallel Port JTAG Emulator along with the key features.

1.0 Overview of the SPI515

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate between +0.8 volts to +5 volts. This emulator is powered from an external power supply which is included with the emulator. This means no power is drawn from the target system.

The SPI515 emulator automatically adjusts to the voltage level of the logic that it will be controlling.

The SPI515 is designed to be compatible with the existing Texas Instruments XDS510 emulator and operate with debuggers provided by Texas Instruments.

1.1 Key Features of the SPI515

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator has the following features:

- Supports Texas Instrument's Digital Signal Processors and Microcontrollers with JTAG interface (IEEE 1149.1)

- Compatible with Texas Instrument's XDS510 emulator.

- Advanced emulation controller provides high performance.

- Supports standard parallel communication interface with host PC (SPP8, EPP, and ECP). No adapter required.

- Supports JTAG interfaces from 1-5 volts.

- Six status LEDs for operational status.

- Incorporates EMU0/EMU1 Wait-In-Reset features for TMS27xx DSPs.

- High speed data logging support over EMU0/1 pins.

- 4 bits of user programmable I/O with variable voltage.

- Power provided by supplied power supply.

- Supports the Texas Instruments Code High Level Language 'C' Debugger

- Compatible with Texas Instruments Code Composer Studio

1.2 Key Items on the SPI515

Figure 1-1 shows the SPI515. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- Programmable I/O interface
- DB-25 connector to the host adapter card
- Power connector

Figure 1-1, KEY ITEMS ON THE SPI515
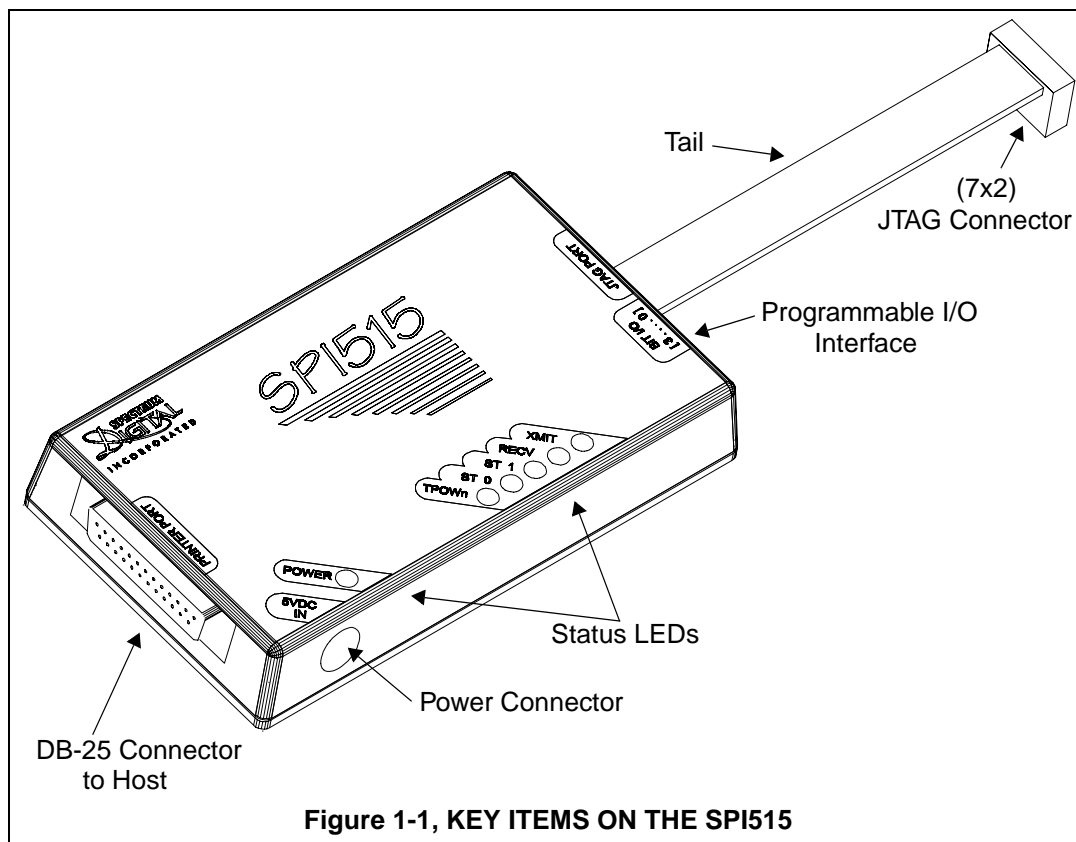
Chapter 2

Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator

This chapter helps you install the SPI515 Adjustable Voltage Parallel Port JTAG Emulator. For use with specific software packages such as the Code Composer Studio or TI HLL debugger refer to their respective documentation.

2.1   What You'll Need

The following checklists detail items that are shipped with the SPI515 and additional items you'll need to use these tools.

Hardware checklist

__	**host**	An IBM PC/AT or 100% compatible PC or laptop with a hard-disk system and a 1.44M floppy-disk drive with SPP8, EPP, or ECP compatible parallel port
__	**memory**	Minimum of 32MB
__	**display**	Color VGA or LCD
__	**emulator module**	SPI515 Adjustable Voltage Parallel Port JTAG emulator with power supply
__	**target system**	A board with a TI DSP or Microcontroller and power supply
__	**connector to target system**	14-pin connector (two rows of seven pins) --- see Chapter 3 for more information about this connector

Software checklist

__	**operating system**	Win 95, Win 98, or Win NT 4.0
__	**software tools**	Compiler/assembler/linker for DSP or Microcontroller
__	**debugger**	Code Composer Studio or TI HLL Debugger
__	**drivers** [t]	drivers for TI Code Composer

[t] Included as part of the SPI515 package

2.2 Voltage Selection

The SPI515 automatically adjusts to the voltage level of the logic that it will be controlling. Table 1 below shows the 18 input and output voltage levels, and target system voltages that will be used. There will be some range overlap due to cable length, noise, etc.

The Signal Output Voltage is the voltage level on the TMS, TDI, TCK, and TRST pins.

The Signal Input Threshold is the voltage level on the TCK_RET, TDO, EMU0, and EMU1 pins.

WARNING !

The Power Detect Input Threshold is the voltage level on the PD pin.

Table 1: Voltage Selection

Signal Output Voltage	Power Detect Threshold	Signal Input JTAG Threshold	Target System Voltage (PD Pin
0.900	0.540	0.540	0.83 - 0.97
1.000	0.600	0.570	0.93 - 1.07
1.100	0.660	0.630	1.03 - 1.17
1.200	0.720	0.660	1.13 - 1.27
1.300	0.780	0.710	1.23 - 1.37
1.400	0.840	0.730	1.33 - 1.47
1.500	0.900	0.780	1.43 - 1.57
1.600	0.960	0.800	1.53 - 1.67
1.700	1.020	0.850	1.63 - 1.77
1.800	1.080	0.900	1.73 - 1.87
1.900	1.140	0.950	1.83 - 1.97
2.000	1.200	1.000	1.93 - 2.07
2.200	1.320	1.100	2.13 - 2.27
2.400	1.440	1.200	2.33 - 2.47
2.600	1.560	1.300	2.53 - 2.67
2.800	1.680	1.400	2.73 - 2.87
3.000	1.800	1.500	2.93 - 3.07
3.200	1.920	1.600	3.13 - 5.00

2.3 Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator

This section contains the steps for installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator.

WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the DB-25 connector while the PC is powered up.
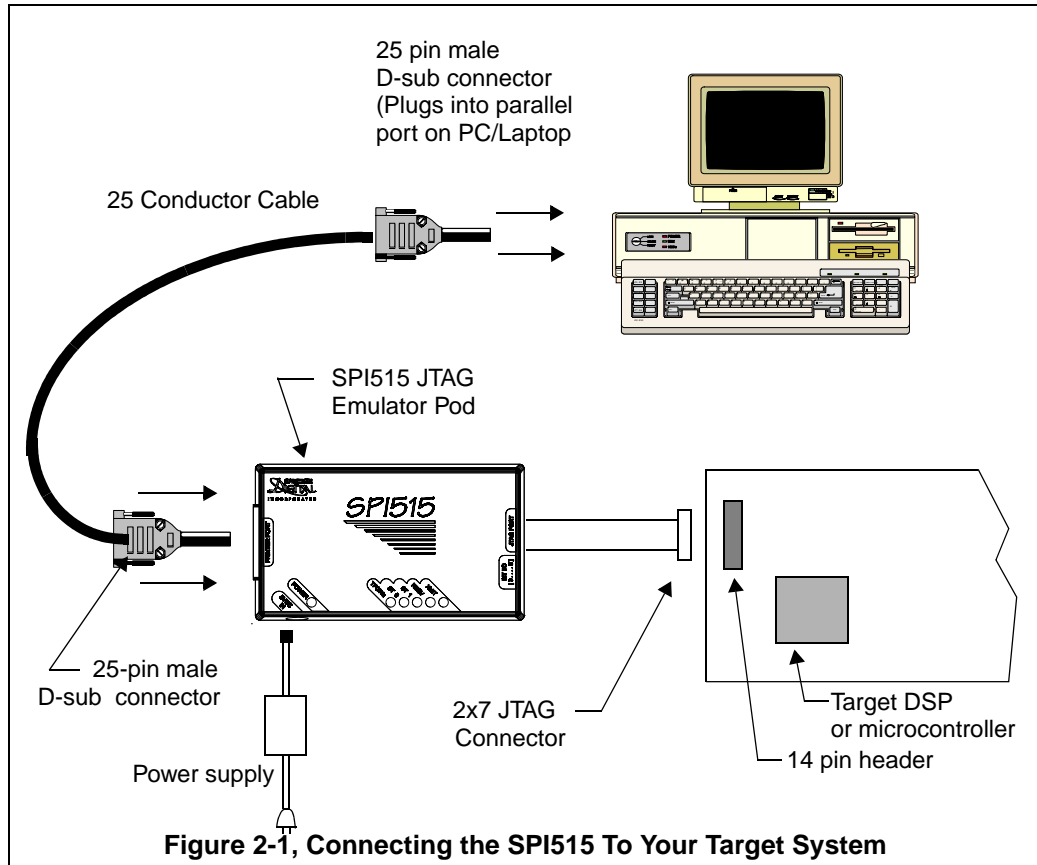
Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

2.3.1 SPI515 Installation Checklist

To install the SPI515 execute the following checklist:

❏ Turn off the power to your PC or laptop

❏ Turn off the power to your target system (DSP or microcontroller system)

❏ Attach the SPI515 DB-25 connector to the parallel port on the PC or laptop with the supplied cable.

❏ Plug power supply for the SPI515 emulator into the emulator.

❏ Plug power supply for the SPI515 emulator into a 110/220 VAC outlet.

❏ Your system configuration should now look like that in Figure 2.1

❏ Apply power to your target.

❏ Apply power to your PC or laptop.

Figure 2-1 shows how you connect the SPI515 in a typical system configuration with a host PC and target board.

25 pin male
D-sub connector
(Plugs into parallel
port on PC/Laptop

25 Conductor Cable

SPI515 JTAG
Emulator Pod

SPI515

25-pin male
D-sub connector

2x7 JTAG
Connector

Power supply

Target DSP
or microcontroller

14 pin header

Figure 2-1, Connecting the SPI515 To Your Target System

2.4 SPI515 LEDs

The SPI515 has 6 red Light Emitting Diodes (LEDs). These LEDs provide the user with the status of the emulator. The meaning of each LED is described in the table below.

Table 2: SPI515 LEDs

LED Name	Function
XMIT	Indicates data is being transmitted to the host system
RECV	Indicates data is being received from the host system
ST1	When on it indicates the TRSTn signal is low
ST0	When on indicates EMU0 signal is low (for WAIT-IN-RESET)
TPOWn	Indicates target power has dropped below input threshold
Power	Indicates power has been applied to the SPI515 emulator

2.5 WAIT-IN-RESET

Newer TI DSPs (e.g. TMS320C27x) have a feature called Wait-In-Reset. When the SPI515 detects the loss of target poser it will drive EMU0 to 0 volts. When the target system is powered on and EMU0 = 0 volts, EMU1 = Vcc, and TRSTn = 0 volts then the DSP will wait in reset until the debugger is started. On processors that do not support Wait-In-Reset" pulling EMU0 should have no effect. EMU0 is tri-stated within 20 milliseconds after TRST returns high. A 100 ohm resistor is included in the event that the target system is driving this signal. Normally this signal is pulled high on the target system with a 4.7K ohm or larger resistor.

Chapter 3

Specifications For Your Target System's Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14-pin connector for proper communication with the emulator.

3.1 Designing Your Target System's Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin header 2 rows of 7 pins) with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-1, 14 Pin Header Signals and Dimensions

Table 1: 14-Pin Header Signal Description

Signal	Description	Emulator State	Target State
TMS	JTAG test mode select.	Output	Input
TDI	JTAG test data input.	Output	Input
TDO	JTAG test data output.	Input	Output
TCK	JTAG test clock. TCK is a 10-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
TRST-	JTAG test reset.	Output	Input
EMUO	Emulation pin 0.	I/O	I/O
EMU1	Emulation pin 1.	I/O	I/O
PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor's I/O pins Vcc.	Input	Output
TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output

Although you can use other headers, recommended parts include:

straight header, unshrouded   DuPont Connector Systems
                                 part # 67996-114

right-angle header, unshrouded   DuPont Connector Systems
                                 part # 68405-114

3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

__ The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

__ The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

3.3 Emulator Cable Pod Logic

Figure 3-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

__ Signals TMS and TDI are generated from the rising edge of TCK_RET.

__ Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.

__ A 10-MHz test clock source is provided. You may also provide your own test clock for greater flexibility.

Figure 3-2, Emulator Pod Interface
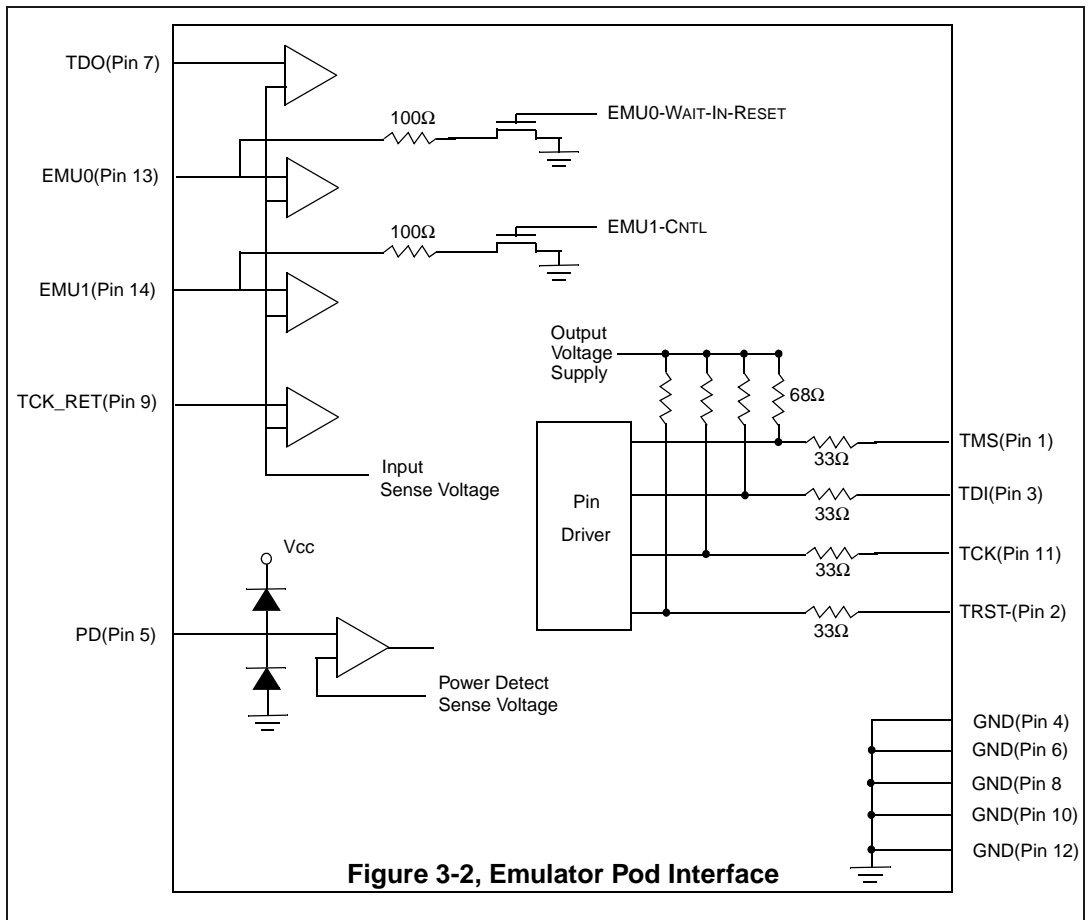
3.4 Emulator Cable Pod Signal Timing

Figure 3-3 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test or guarantee these timings.
The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.
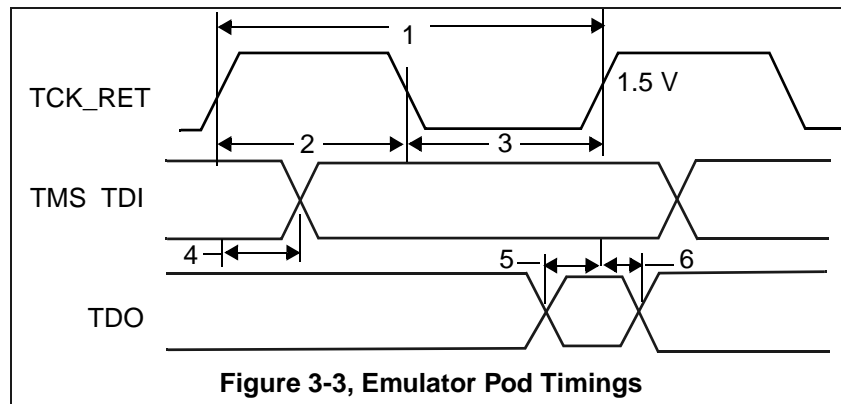

Figure 3-3, Emulator Pod Timings

Table 2: Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	50	10000	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	15		ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	15		ns
4	$td_{(XTMX)}$	TMSFTDI valid from TCK_RET high	20	35	ns
5	$tsu_{(XTDOmin)}$	TDO setup time to TCK_RET high	10		ns
6	$thd_{(XTDOmin)}$	TDO hold time from TCK_RET high	4		ns

3.5 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

— **No signal buffering.** As shown in figure 3-4, the distance between the header and the target device should be no more than 6 inches.
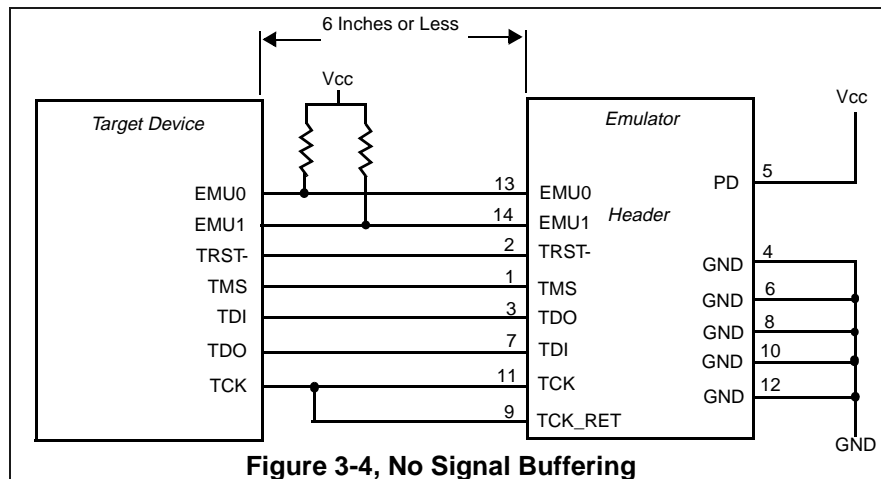
Figure 3-4, No Signal Buffering

— **Buffered emulation signals.** Figure 3-5 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.
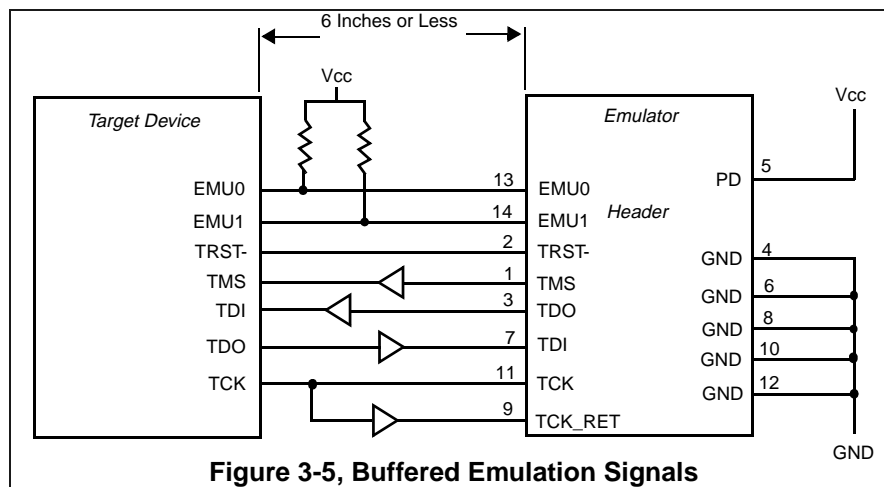
Figure 3-5, Buffered Emulation Signals

___ The EMU0 and EMU1 signals must have pullups to Vcc. The pullup resistor value should be chosen to provide a signal rise time less than 10 uS. A 4.7k ohm resistor is suggested for most applications. EMUO-1 are I/O pins on the target device, however, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.

___ It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 3-6 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.

Figure 3-6, Target System Generated Test Clock
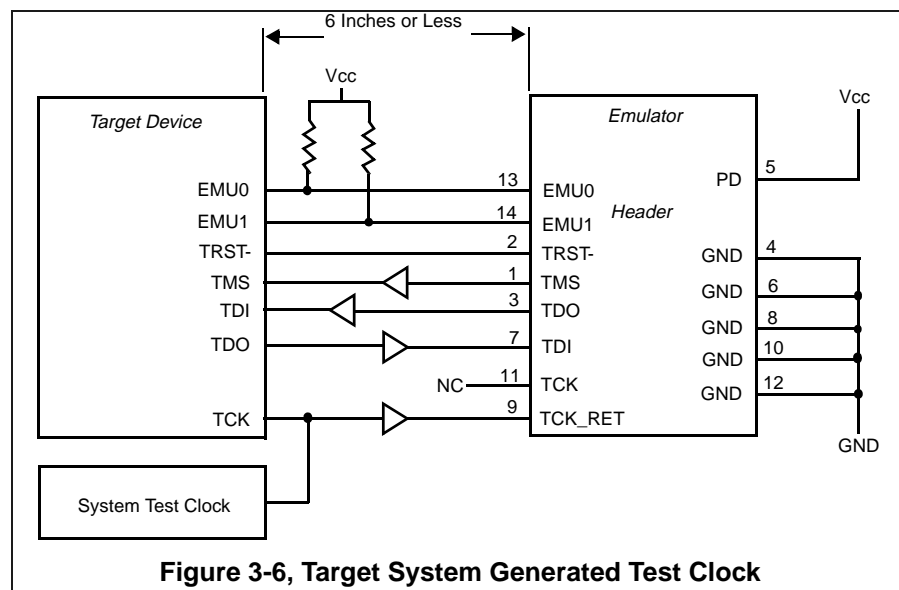
There are two benefits to having the target system generate the test clock:

___ The emulator provides only a single 10-MHz test clock. If you generate your own test clock, you can set the frequency to match your system requirements.

___ In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.
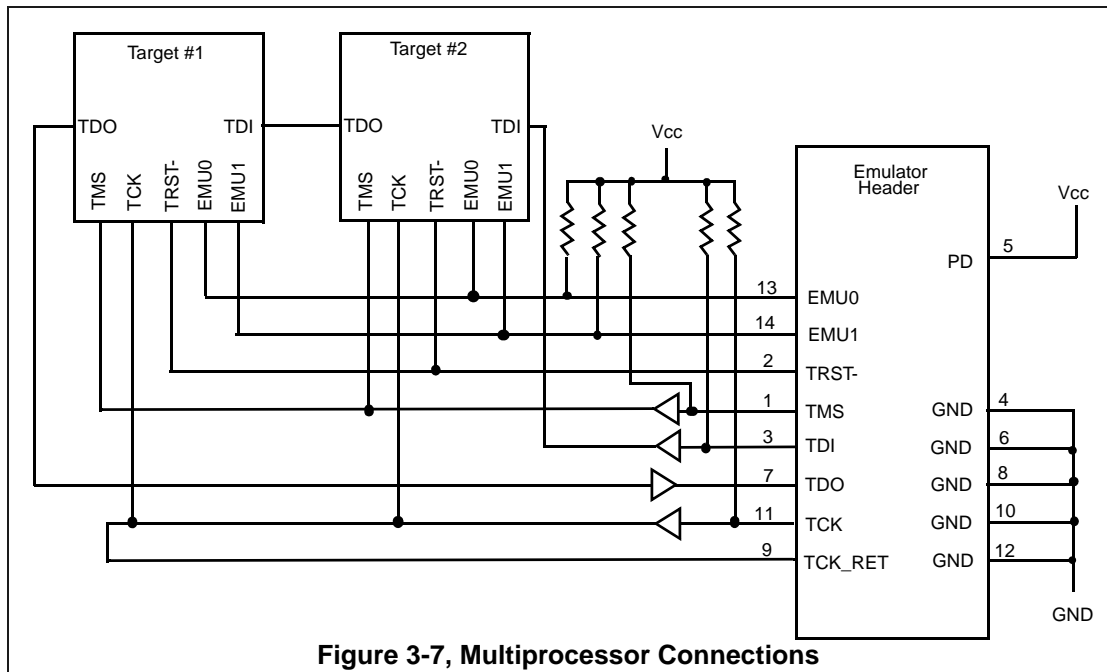
Figure 3-7, Multiprocessor Connections

Figure 3-7 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multiprocessor support are as follows:

___ The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.

___ The input buffers for TMS, TDI, and TCK should have pullups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pullup of 4.7k ohms or greater is suggested.

3.6 Emulation Timing Calculations

The following are a few examples on how to calculate the emulation timings in your system. For actual target timing parameters, see the appropriate device data sheets.

Assumptions:

$t_{su(TTMS)}$	Target TMS/TDI setup to TCK high	10	ns
$t_{h(TTMS)}$	Target TMS/TDI hold from TCK high	5	ns
$t_{d(TTDO)}$	Target TDO delay from TCK low	15	ns
$t_{d(bufmax)}$	Target buffer delay maximum	10	ns
$t_{d(bufmin)}$	Target buffer delay minimum	1	ns
$t_{(bufskew)}$	Target buffer skew between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}]$ x 0.15	1.35	ns
$t_{tckfactor}$	Assume a 40/60 duty cycle clock	0.4	

Given in Table 2:

$t_{d(XTMSmax)}$	Emulator TMS/TDI delay from TCK_RET high, max	35	ns
$t_{d(XTMXmin)}$	Emulator TMS/TDI delay from TCK_RET high, minimum	20	ns
$t_{su(XTDOmin)}$	TDO setup time to emulator TCK_RET high	10	ns

There are two key timing paths to consider in the emulation design:

___ the TCK_RET/TDI(t_{prdtck_TMS}) path, and
___ the TCK_RET/TDO(t_{prdtck_TDO}) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.

Case 1: Single processor, direct connection, TMS/TDI timed from TCK_RET high.

t_{prdtck_TMS} $= t_{d(XTMSmax)} + t_{su(TTMS)}$
$= (35ns + 10ns)$
$= 45ns\ (22.2\ MHz)$

t_{prdtck_TDO} $= [t_{d(TTDO)} + t_{su(XTDOmin)}] / t_{tckfactor}$
$= (15ns + 10ns) / 0.4$
$= 62.5ns\ (16.0\ MHz)$

In this case, the TCK/TDO path is the limiting factor. One other thing to consider in this case is the TMS/TDI hold time. The minimum hold time for the emulator cable pod is 20ns, which meets the 5ns hold time of the target device.

Case 2: Single/multiple processor, TMS/TDI buffered input; TCK_RET/TDO buffered output, TMS/TDI timed from TCK_RET high.

t_{prdtck_TMS} $= t_{d(XTMSmax)} + t_{su(TTMS)} + 2t_{d(bufmax)}$
$= (35ns + 10ns + 2(10ns)$
$= 65ns\ (15.3\ MHz)$

t_{prdtck_TDO} $= (t_{d(TTDO)} + t_{su(XTDOmin)} + t_{bufskew}) / t_{tckfactor}$
$= (15ns + 10ns + 1.35\ ns) / 0.4$
$= 65.8ns\ (15.1\ MHz)$

In this case, the TCK/TDO path is the limiting factor. The hold time on TMS/TD is also reduced by the buffer skew (1.35 ns) but still meets the minimum device hold time.

3.7 Mechanical Dimensions of the SPI515 Adjustable Voltage JTAG Emulator

The SPI515 Adjustable Voltage Scan Path Interface Pod consists of a 3-foot 25 conductor cable, the **SPI515** emulator pod, and a short section of cable that connects to the target system. The overall cable length is approximately 3 feet, 10 inches. Figure 3-8 and Figure 3-9 (page 3-12) show the mechanical dimensions for the **SPI515** emulator pod and short cable. Note that the pin-to-pin spacing on the connector is 0.100 inches in both the X and Y planes. The **SPI515** enclosure is nonconductive plastic with four recessed metal screws.
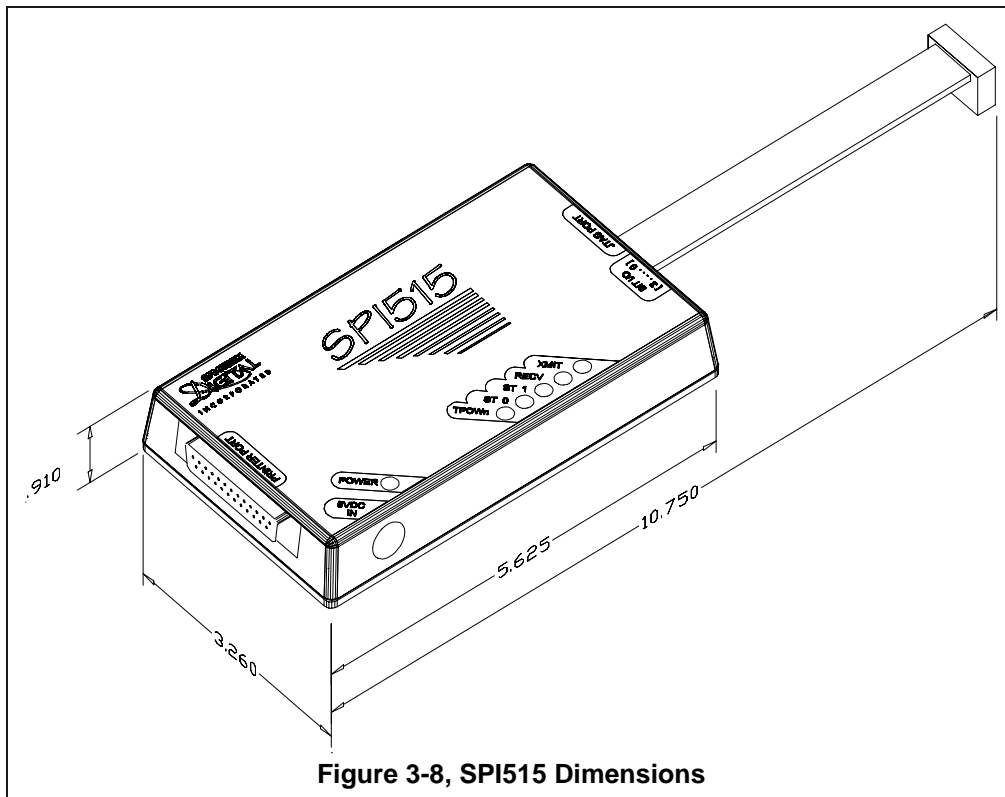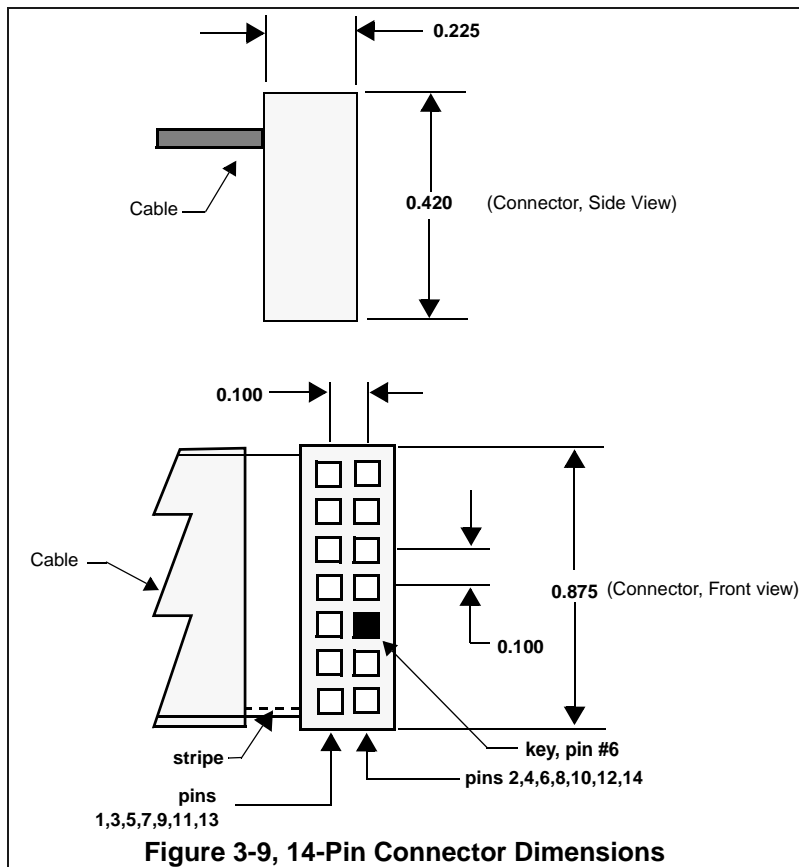

Figure 3-8, SPI515 Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

Figure 3-9, 14-Pin Connector Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

Chapter 4

Specifications For Your Target's I/O Interface to the Emulator

This chapter contains information about connecting your target system's logging interface to the SPI515 emulator. Your target system must use a special 10-pin connector for proper communication with the emulator.

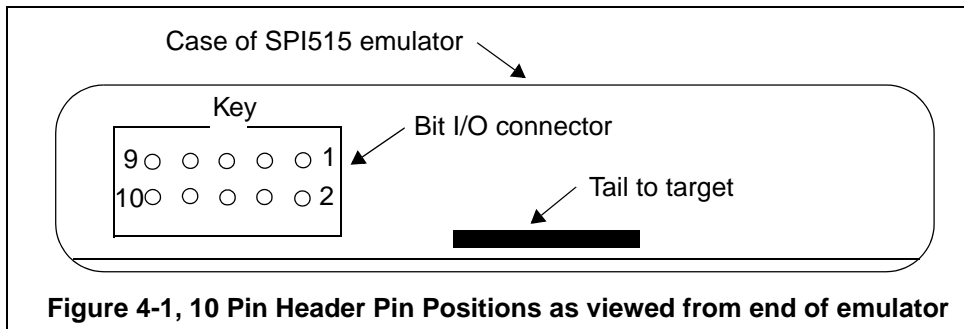**4.1 Designing Your Target System's Logging Connector (10-pin Header)**

The SPI515 has a 10 pin header for bit I/O support and SPI515 data logging. When used for data logging all the bit I/O pins are used. The SOMI pin drives a constant level in version 3 and earlier of the SPI515. There is no slave-to-master channel. The DSP is the master and the SPI515 is the slave. The maximum SCLK is 20 Mhz. SIMO data should be driven by the master on the rising edge of SCLK with no delay. The SPI515 captures data on the falling edge of SCLK.

The table below shows the signals on the logging connector.

Table 1:

Pin #	Signal	Pin #	Signal
1	BitI/O-0,STE(input)	2	GND
3	BitI/O-1,SIMO(input)	4	GND
5	BitI/O-2, SCLK(input)	6	GND
7	BitI/O-3, SOMI(output)	8	GND
9	NC	10	NC

The figure below shows the logging connector on the emulator as viewed from the end. The position of the pins is indicated. The connector on the SPI515 is a male connector and keyed above pin 5.
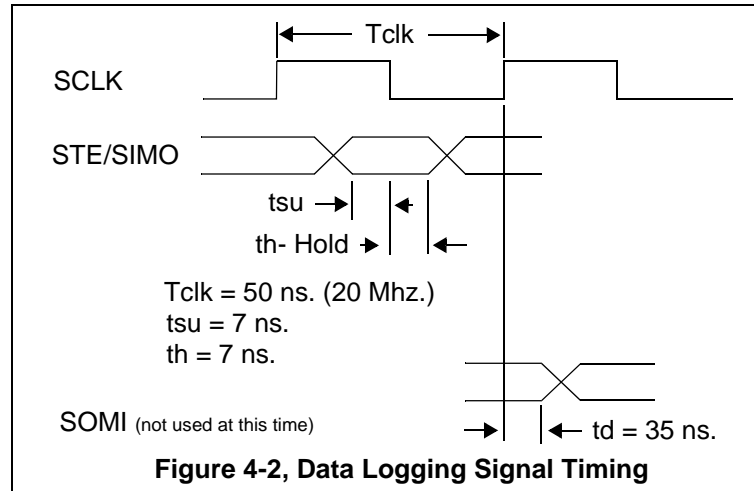
Case of SPI515 emulator

Key

Bit I/O connector

9 ○ ○ ○ ○ ○ 1
10○ ○ ○ ○ ○ 2

Tail to target

Figure 4-1, 10 Pin Header Pin Positions as viewed from end of emulator

Although you can use other headers, recommended parts include:

header, unshrouded   AMP #: 746286-1

4.2 Data Logging Signal Timing

The signal timing for the data logging on the Bit I/O connector is shown below.

SCLK

STE/SIMO

tsu

th- Hold

Tclk = 50 ns. (20 Mhz.)
tsu = 7 ns.
th = 7 ns.

SOMI (not used at this time)   td = 35 ns.

Figure 4-2, Data Logging Signal Timing

4.3 Data Logging Circuitry

The circuit logic for the Bit I/O 0,1,2, and 3 on the Bit I/O connector is shown below.

Input Sense

Bit I/O (0..3)

Output voltage supply

4.7K

Zcntl

Figure 4-3, Data Logging Circuit Logic
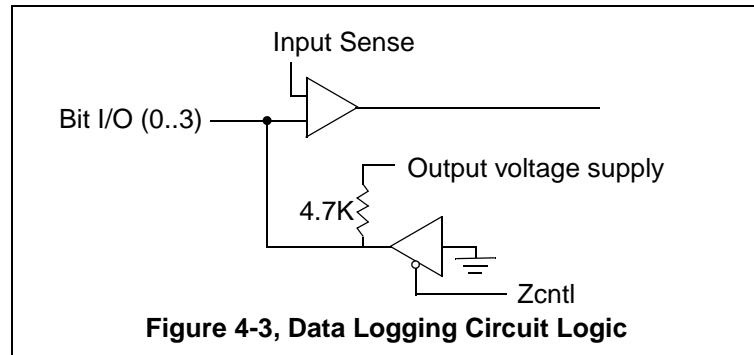
• Input/Output levels are derived from the JTAG PD pin shown in table 1.

• Pins used for data logging cannot be used for Bit I/O.

• Output pins behave as open collector. For faster rise time on output turn off, the user may include a pullup resistor with connection to the same power supply that sources the JTAG PD pin. The minimum external pullup is 100 ohms.

4.4 Data Logging Connections
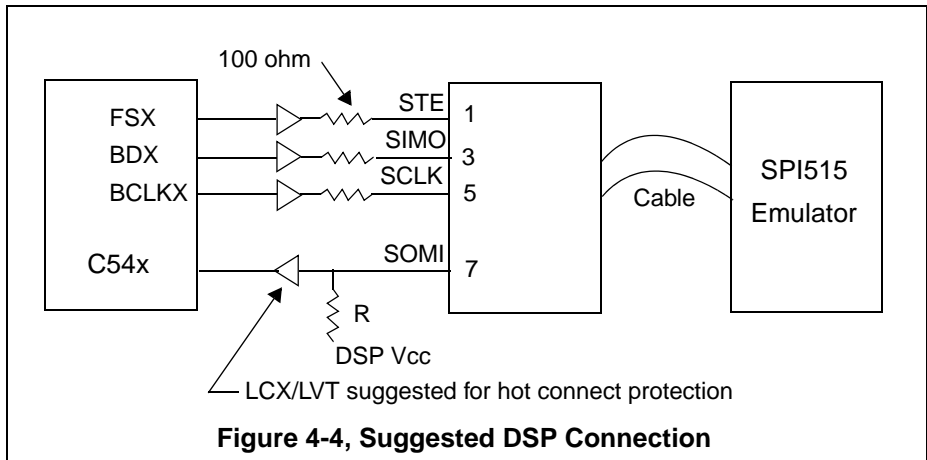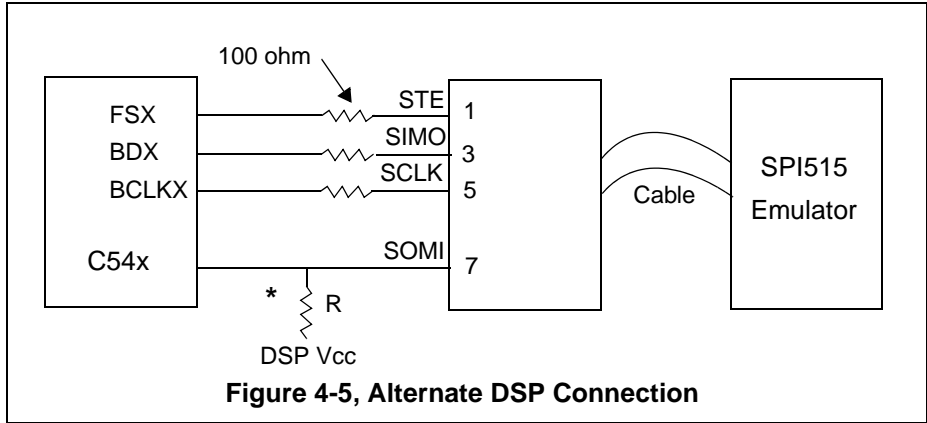
Figure 4-4 below shows the suggested DSP connection.

Figure 4-4, Suggested DSP Connection

Figure 4-5 below shows an alternate DSP connection.

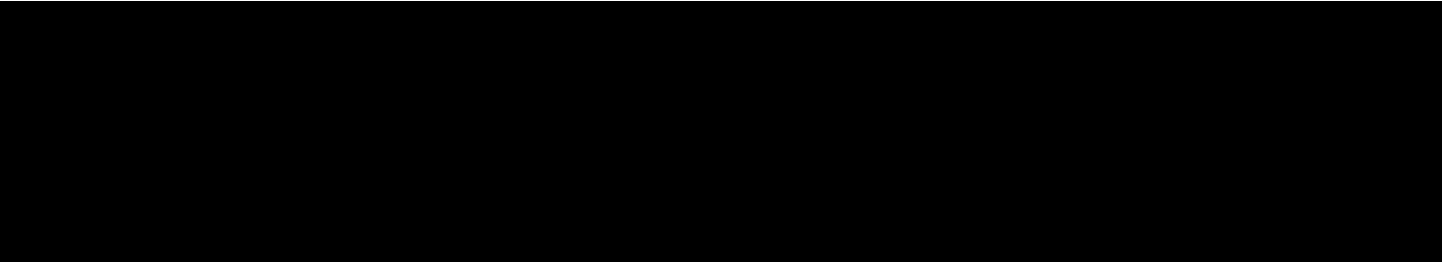**Figure 4-5, Alternate DSP Connection**

* If future support is required:

    R = 1K ohm typical

    R may be lowered to increase SCLK frequency.

    Output pins behave as open collector. For faster rise time on output turn off, the user may include a pullup resistor with connection to the same power supply that sources the JTAG PD pin. The minimum value of R, the external pullup is 100 ohms with DSP Vcc = 3.6 volts.

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