SPECTRUM DIGITAL INCORPORATED

TMS320VC5416 DSK

Technical Reference

2002 DSP Development Systems

TMS320VC5416 DSK
Technical Reference

506005-0001 Rev. A
March 2002

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5416 DSP Starter Kit (DSK) module. The DSK is based on the Texas Instruments TMS320VC5416 Digital Signal Processor.

The TMS320VC5416 DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5416 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5416 will sometimes be referred to as the C54XX.

The TMS320VC5416 DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC54XX Users Guide
Texas Instruments TMS320VC54XX Fixed Point Assembly Language Users Guide
Texas Instruments TMS320VC54XX Fixed Point C Language Users Guide
Texas Instruments TMS320VC54XX Code Composer Studio Users Guide

Table 1: Hardware History

Revision	History
B	Beta Release
C	Production Release

Table 2: Manual History

Revision	History
A	Beta Release

Chapter 1

Introduction to the TMS320VC5416 DSK

Chapter One provides a description of the TMS320VC5416 DSK along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320VC5416 DSK

The TMS320VC5416 DSK is a stand-alone development and evaluation module. It allows evaluators to examine certain characteristics of the C5416 digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320VC5416 family of processors.

The DSK allows full speed verification of VC5416 code. With 64K words of on board RAM memory, 256K words of on board Flash ROM, and a Burr Brown PCM 3002 stereo codec, the board can solve a variety of problems as shipped. Three expansion connectors are provided for interfacing to evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a special version of Code Composer Studio is shipped with the board.

1.1 Key Features of the TMS320VC5416 DSK

The VC5416 DSK has the following features:

- VC5416 operating at 16-160 MHz.
- On board USB JTAG controller with plug and play drivers
- 64K words of on board RAM
- 256K words of on board Flash ROM
- 3 Expansion Connectors (Memory Interface, Peripheral Interface, and Host Port Interface)
- On board IEEE 1149.1 JTAG Connection for Optional Emulation Debug
- Burr Brown PCM 3002 Stereo Codec
- +5 volt operation

1.2 Functional Overview of the TMS320VC5416 DSK

Figure 1-1 shows a block diagram of the basic configuration for the VC5416 DSK. The major interfaces of the DSK include the target RAM and ROM interface, FPGA interface, Codec interface, and expansion interface.

The VC5416 interfaces to 64K words of on board RAM and 256K words of Flash ROM. An external I/O interface supports parallel I/O ports and multi channel buffered synchronous serial ports. A Flash Boot ROM is mapped into data memory space. Four stereo jacks provide input and outputs to and from the codec.

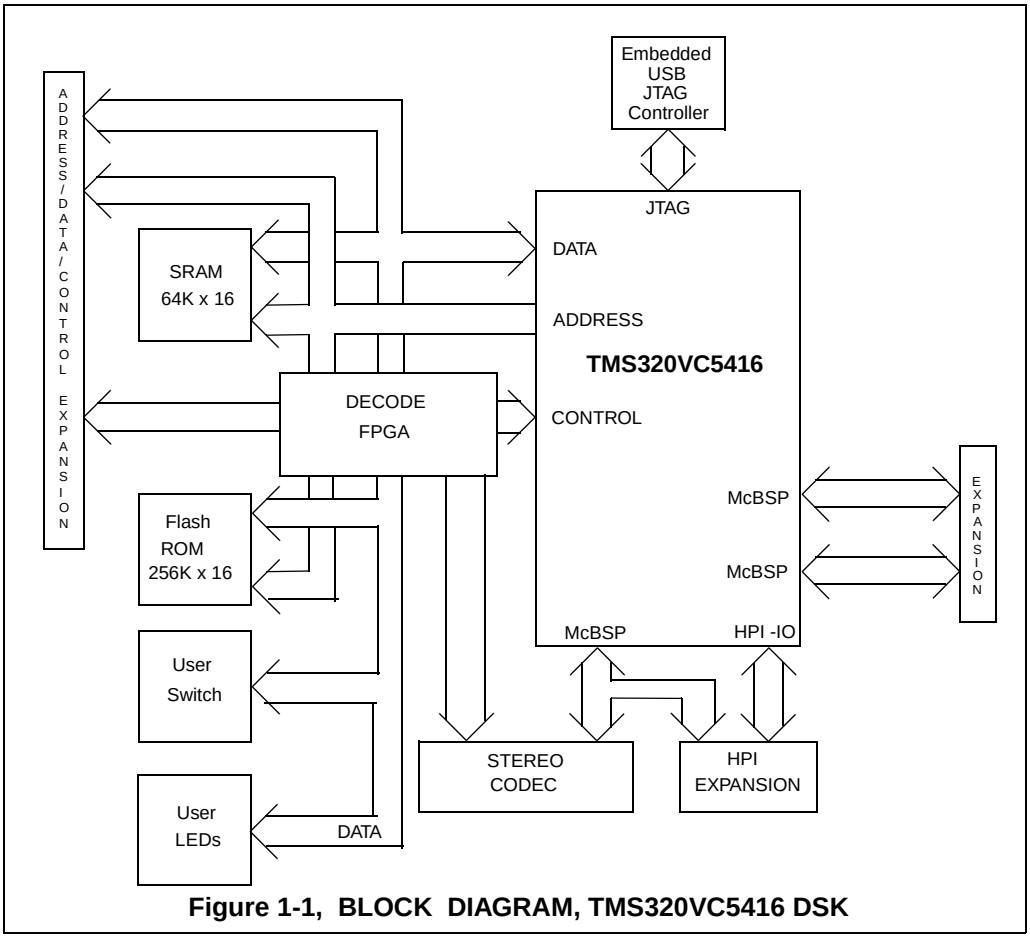

Figure 1-1, BLOCK DIAGRAM, TMS320VC5416 DSK

Chapter 2

Operation of the TMS320VC5416 DSK

This chapter describes the operation of the TMS320VC5416 DSK, the key interfaces and an outline of the circuit board.

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2.0 The TMS320VC5416 DSK Operation

This chapter describes the VC5416 DSK module, key components, and how they operate. It also provides information on the DSK's various interfaces.The VC5416 DSK consists of five major blocks of logic.

- C5416 External memory
- Codec Interface
- CPLD Registers and Interface
- Expansion interface
- JTAG Interface

2.1 The TMS320VC5416 DSK Board

The VC5416 DSK is a 8.25 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 2-1 shows the layout of the VC5416 DSK.

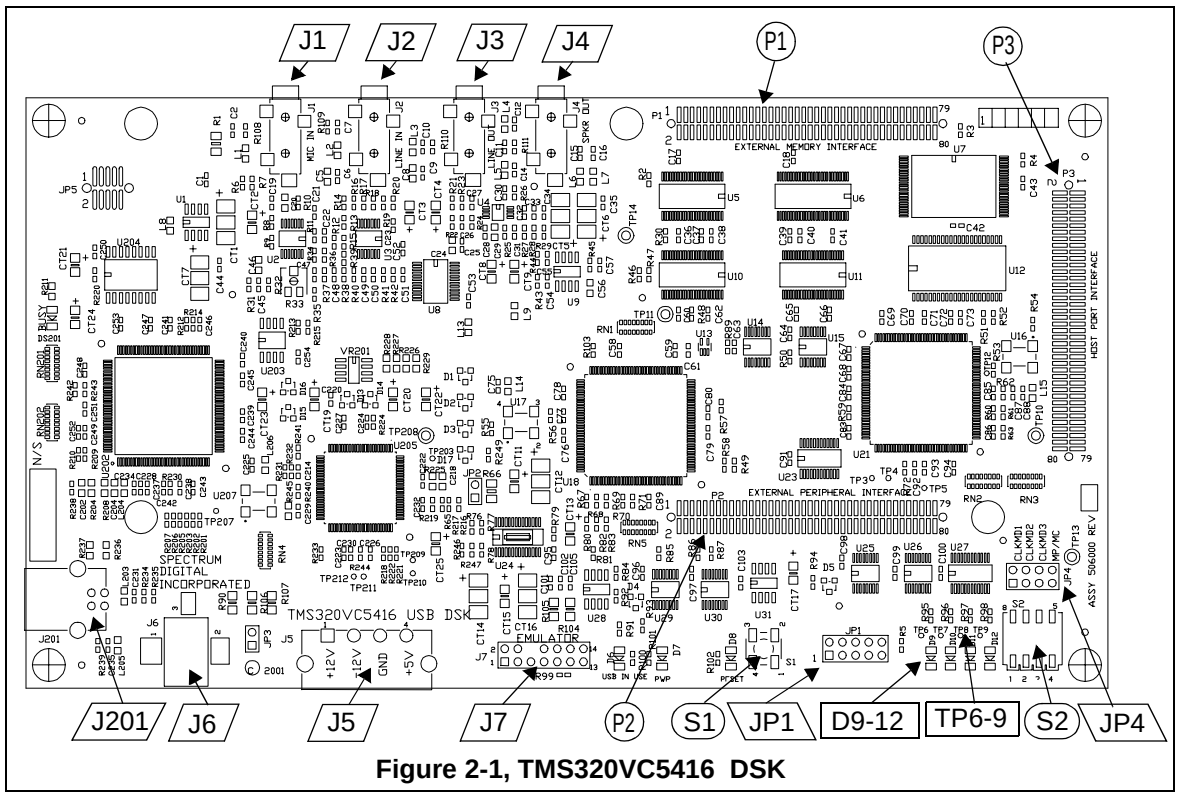


Figure 2-1, TMS320VC5416 DSK

2.1.1 Power Connector

The VC5416 DSK is powered by a +5 volt only, 3 amp power supply which is available with the module. The typical board current requirements, without expansions boards, is 0.5 - 0.75 amps. The power is supplied via 2.5 millimeter jack JP6. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board also has a +3.3 and +1.6 volt regulator to provide power to the lower voltage components.

2.2 TMS320C5416 DSK Memory Interface

The DSK includes 64K words of SRAM. The board also features 256K words flash ROM for boot loading.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your DSK card please refer to Texas Instruments TMS320C54XX Users Guide or TMS320VC5416 data sheet. Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Software Wait State Generation Register(SWWSR). To obtain wait states for off-chip memory, bits in the SWWSR must be appropriately programmed. The board powers up with maximum wait-states. The DSK board does not generate wait states via the ready signal for external program memory, data memory, or I/O accesses.

External memory decode is done via CPLD U8. The complex program logic device selects the RAM, FLASH ROM, or on board peripherals. The VHDL for the CPLD are included in Appendix A.

The internal PMST register (Processor Mode Status Register) greatly affects the memory decode for the VC5416 and VC5416 DSK. The user should be familiar with this register to help in the understanding of the DSK's operation. The figure below shows the bit fields of the PMST register and a brief description of the register's function bits.

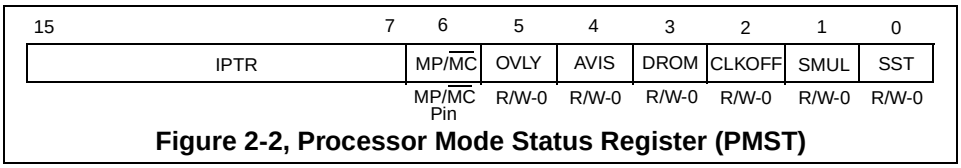


Figure 2-2, Processor Mode Status Register (PMST)

The bit fields in PMST are described in the table below.

Table 1: PMST Bit Field Definition

Bit #	Bit Name	Reset Value	Function
15-7	IPTR	1FFh	Interrupt vector pointer - The 9-bit IPTR field points to the 128-word program page where the interrupt vectors reside. The interrupt vectors can be remapped to RAM for boot-loaded operations. At reset, these bits are all set to 1; the reset vector always resides at address FF80h in the program memory space. The RESET instruction does not affect this field.

Table 1: PMST Bit Field Definition

Bit #	Bit Name	Reset Value	Function
6	MP/$\overline{MC}$	MP/$\overline{MC}$ Pin	Microprocessor/microcontroller Mode - MP/$\overline{MC}$ enables/ disables the on-chip ROM to be addressable in program memory space. - MP/$\overline{MC}$ = 0: The on-chip ROM is enables and addressable. - MP/$\overline{MC}$ = 1: The on-chip ROM is not addressable. MP/$\overline{MC}$ is set to the value corresponding to the logic level on the MP/MC pin when samples at reset. This pin is not samples again until the next reset. The RESET instruction does not affect this bit. This can also be set or cleared by software.
5	OVLY	0	RAM overlay. OVLY enables the on-chip dual address dual-access data RAM blocks to be mapped into program space. The values for the OVLY bit are: - OVLY = 0: The on-chip RAM is addressable in data space but not in program space. - OVLY = 1: The on-chip RAM is mapped into program space and data space. Data page 0 (address 0h to 7Fh)., however it not mapped into program space.
4	AVIS	0	Address visibility mode. AVIS enables/disables the internal program address to be visible at the address pins. - AVIS = 0: The external address lines do not change with the internal program address. control and data lines are not affected and the address bus is driven with the last address on the bus. - AVIS = 1: This mode allows the internal program address to appear at the pins of the 5416 so that the internal program address can be traced. Also, it allows the interrupt vector to be decoded in conjunction with IACK when the interrupt vectors reside in-chip memory.

Table 1: PMST Bit Field Definition

Bit #	Bit Name	Reset Value	Function
3	DROM	0	DROM - Enables on-chip DARAM4-7 to be mapped into data space. The DROM values are: - DROM = 0: The on-chip DARAM4-7 is not mapped into data space - DROM = 1: The on-chip DARAM4-7 is mapped into data space
2	CLKOFF	0	CLKOUT off. When the CLKOFF bit is a 1, the output of the CLKOUT is disabled and remains at a high level
1	SMUL	N/A	Saturation on multiplication. When SMUL = 1, saturation of a multiplication result occurs before performing the multiplication in a MAC or MAS instruction. The SMUL bit applies only when the OVM=1 and FRCT=1.
0	SST	N/A	Saturation on store. When SST = 1, saturation of the data from the accumulator is enabled before storing in memory. The saturation is performed after the shift operation

2.2.1 Program Memory Interface

There are two configurations for program memory. The selection of these configurations is done by the 54X's OVLY bit. When in OVLY mode, addresses 0x0000 - 0x8000 are internal for every page. This is the preferred mode to be used by the DSK. When in linear mode program memory is mapped externally.

Manual sections 2.2.5 and 2.2.6 show how on-board memory is mapped into the external spaces of the processor.

The following figure shows the program memory map for TMS320VC5416.

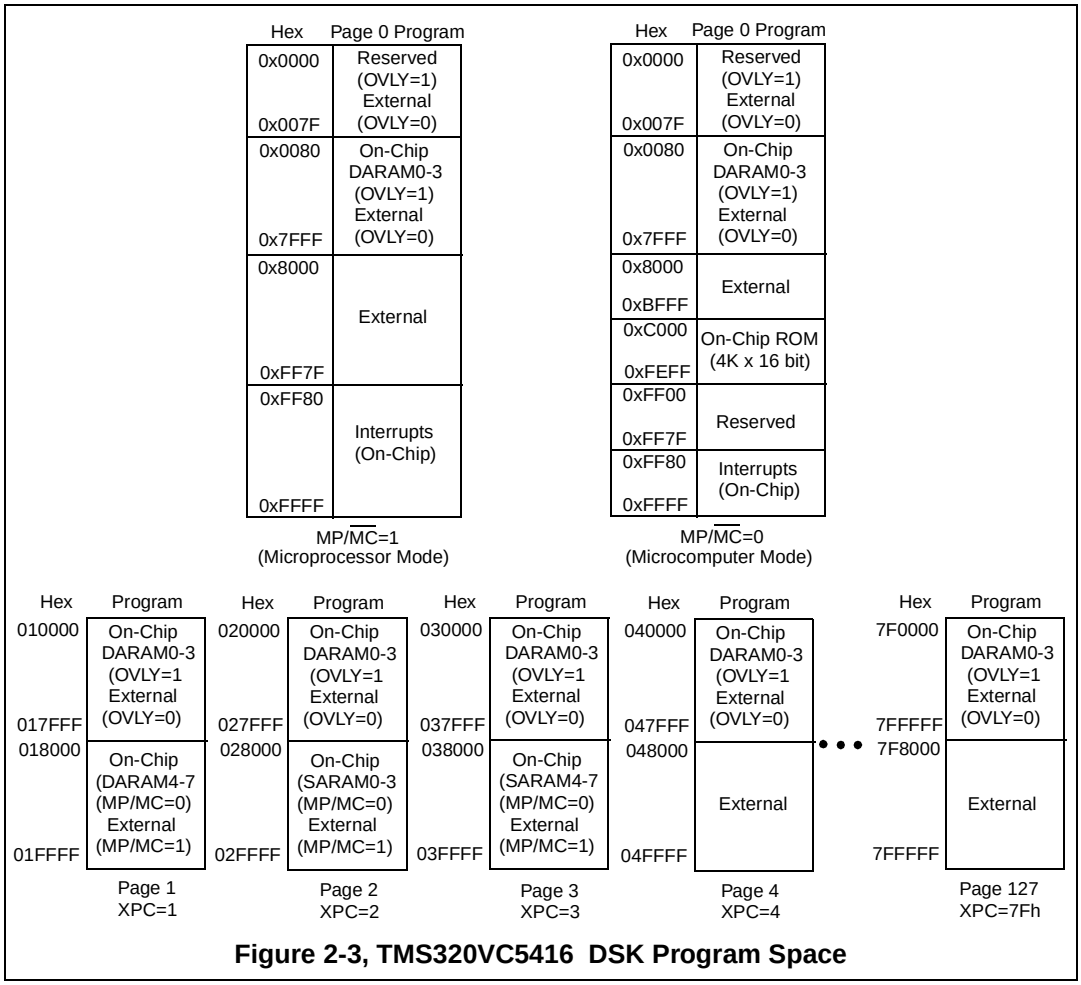


Figure 2-3, TMS320VC5416 DSK Program Space

2.2.2 Data Memory

The external data memory is mapped from 0x8000 to 0xFFFF for the DSK. This allows a reach of 32K words. The on board CPLD further supplies 5 additional address lines to allow for thirty-two (32), 32K word pages to be accessed in data space. All on board accesses are mapped into the processors data memory space from 0x8000 to 0xFFFF and use the extended address lines from the CPLD.

Refer to the section on Data Space Access for how the DSP and CPLD pages address interact. The figure below shows the data space memory map for the TMS320VC5416 processor.

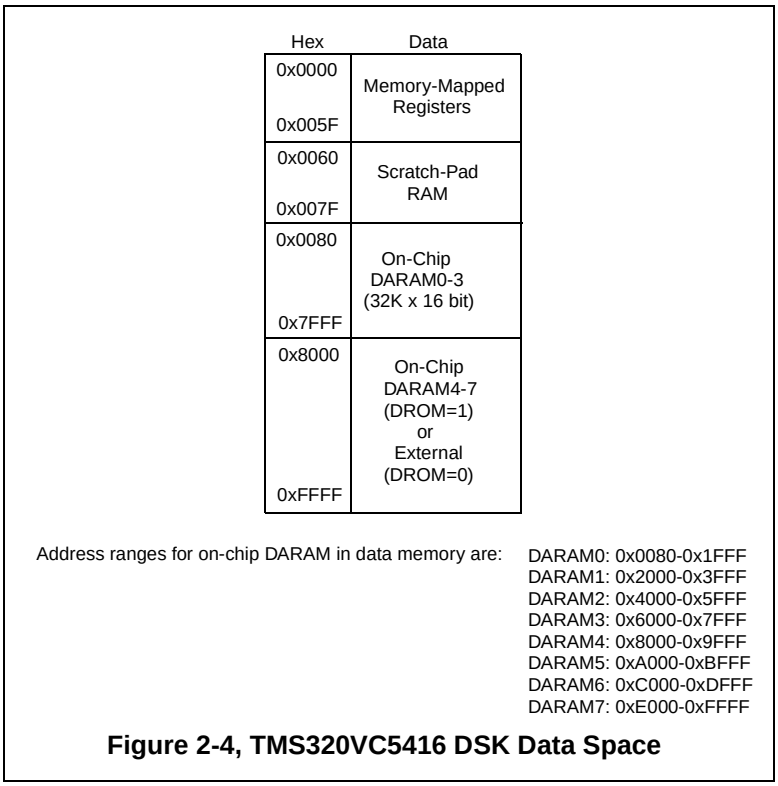


Figure 2-4, TMS320VC5416 DSK Data Space

2.2.3 I/O Space

The TMS320VC5416 processor has no on-chip I/O accesses. The DSK uses this space to access the on board CPLD and expansion connectors for daughter card accesses.

The I/O map for the TMS320VC5416 DSK is shown below. The CPLD has eight (8) 8 bit registers which control various functions as explained in the “Interface CPLD” section of this manual.

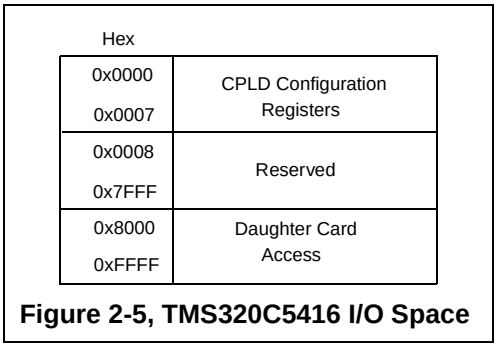


Figure 2-5, TMS320C5416 I/O Space

2.2.4 Interface CPLD

The VC5416 uses a CPLD to interface to the Flash ROM, SRAM, Codec control, and the Daughter Card Interface. The CPLD is mapped into the I/O address space and contains eight (8) 8-bit registers as shown below.

2.2.4.1 CPLD Control Registers and Status Registers

There are eight DSP CPLD registers mapped into the DSP's lower I/O address space starting at address 0x0000 to 0x0007. Since the CPLD decoder only uses part of the DSP's Address for decoding, the registers will be mirrored within the I/O space addresses in 64 word increments within the lower 16K of the I/O address space. It is recommended that the CPLD registers only be accessed at locations 0x0000 to 0x0007 so future implementations will not case software changes.

The table below shows the bit definitions for the 8 registers in CPLD.

Table 2: CPLD Register Definitions

I/O Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W	USR_LED2 R/W	USR_LED1 R/W	USR_LED0 R/W
1	DC_REG	DC_DET R	DC_IO_CTL R/W 0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(on reset)	0	DC_CNTL1 R/W 0(low)	DC_CNTL0 R/W 0(low)
2	CODEC_L	CODEC_L_CMD[7..0] R/W 0							
3	CODEC_H	CODEC_H_CMD[15..8] R/W 0							
4	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
5	DM_CNTL	DM_SEL R/W 0(int)	MEMTYPE_DS R/W 0(flash)	MEMTYPE_PS R/W 0(flash)	DM_PG4 R/W 0(page 0)	DM_PG3 R/W 0(page 0)	DM_PG2 R/W 0(page 0)	DM_PG1 R/W 0(page 0)	DM_PG0 R/W 0(page 0)
6	MISC	CODEC_RDY R 0(Ready)	0	0	0	0	DC_WIDE R/W 0(16 bits)	DC32-ODD R/W 0(even)	BSP2SEL R/W 0(CODEC)
7	CODEC_CLK	0	0	0	0	DIV_SEL R/W	CLK_STOP R/W	CLK_DIV1 R/W	CLK_DIV0 R/W

Note: "**R**" indicates Read Only, "**R/W**" indicate Read and Writable

2.2.4.1.1 DSP USER_REG Register (I/O Address 0x0000)

The USER register controls the status of the 4 user LED's and the state of the 4 Position User DIP Switch. The table below summarizes (bold indicates default) the function of each bit in the USER_REG register.

Table 3: USER_REG Bit Definition

Bit #	Name	R/W	Description
7	USER_SW3	R	User DIP Switch S2-4 (1 = Off, 0=On)
6	USER_SW2	R	User DIP Switch S2-3 (1 = Off, 0=On)
5	USER_SW1	R	User DIP Switch S2-2 (1 = Off, 0=On)
4	USER_SW0	R	User DIP Switch S2-1 (1 = Off, 0=On)
3	USER_LED3	R/W	User Defined LED D12, Control(**0=Off**, 1=On)
2	USER_LED2	R/W	User Defined LED D11, Control(**0=Off**, 1=On)
1	USER_LED1	R/W	User Defined LED D10, Control(**0=Off**, 1=On)
0	USER_LED0	R/W	User Defined LED D9, Control(**0=Off**, 1=On)

2.2.4.1.2 DSP Daughter Card Register (I/O Address 0x0001)

The DC_REG register provides user control of the two daughter card control outputs, the daughter card reset signal, and the status of the two daughter card Status signals and the Daughter Card Detect Signal. The table below summarizes (**bold indicates default**) the function of each bit in the DC_REG register.

Table 4: DC_REG Bit Definitions

Bit #	Name	R/W	Description
7	DC_DET	R	Daughter Card Detection(0=No board, 1=Daughter Card Detected)
6	DC_IO_CTL	R/W	**0=None**, 1=DC_RE-,DC_WE- active on I/O Cycles
5	DC_STAT1	R	Daughter Card Status 1 (0=low, 1=high)
4	DC_STAT0	R	Daughter Card Status 0 (0=low, 1=high)
3	DC_RST	R/W	Daughter Card Reset (1=Reset Active Low)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1 (**0=low**, 1=high)
0	DC_CNTL0	R/W	Daughter Card Control 0 (**0=low**, 1=high)

2.2.4.1.3 DSP CODEC_L_CMD (I/O Address 0x0002) and CODEC_H_CMD Register (I/O Address 0x0003)

This Read/Write register is use to send command codes to the on board Burr-Brown PCM3002 CODEC. The two 8-bit register form the 16 command word that is to be sent to the CODEC. Any read accesses to these two I/O addresses will only read the last command that was written to the CODEC. Write accesses to I/O address 0x0002 will only store the byte into the CODEC_L register. After the completion of a write to I/O address 0x0003, the CPLD will transfer the complete 16-bit command word to the CODEC.

Refer to the PCM3002 data sheet for complete definition of the bits and commands.

NOTE: After each write of CODEC_H register the DSP is required to wait 1 millisecond, before writing any data to either location. The user may poll bit 7 of I/O address 0x06 (MISC Register) to determine if the Codec is Ready, this bit contains the CODEC_RDY- bit. When the CODEC_RDY- is equal to zero (0x0), then a new command can be written to these command registers. When the CODEC_RDY is equal to one (1), then the previous command in still be shifted into the PCM3002 device.

2.2.4.1.4 Version Register (I/O Address: 0x0004)

This register contains two version codes of the DSK. The CPLD version code is the upper 4-bits of this register. The CPLD version code is coded into the device during compilation of the VHDL source. The board version code is read from the lowest 3-bits of this register. The board version is set during board assembly.

Table 5: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	DSK_VER2	R	Most Significant DSK Board Version Bit
1	DSK_VER1	R	DSK Board Version Bit
0	DSK_VER0	R	Least Significant DSK Board Version Bit

2.2.4.1.5 DSP DM_CNTL Register (I/O Address 0x0005)

The DM_CTRL register enables the DSP software to control the data and program memory space selection between external on-board and off-board daughter card memory. This Register also supplies the upper page address bits for data memory accesses. Since the 5416 DSK only provides a 32K window for external data memory 5 additional address bits are supplied by the CPLD, to expand the DSK's data reach.

The DM_SEL bit selects whether accesses to data memory locations at 0x8000 to 0xFFFF are onboard, or whether the accesses select daughter card memory locations.

MEMTYPE_DS selects whether onboard data memory accesses from 0x8000 to 0xFFFF access flash memory (The default at reset to allow the DSP to support parallel booting from on-board FLASH) or whether these accesses select the on-board SRAM. Note that DM_SEL has precedence over MEMTYPE_DS, therefore DM_SEL must be "0" to access on board data memory space.

MEMTYPE_PS selects either Flash in external on board program space (MEMTYPE_PS=0) or SRAM in external on board space (MEMTYPE_PS=1). All external accesses to program space from 0x000000 to 0x3FFFFF access on board memory. Accesses from 0x40000 to 0x7FFFFF access daughter card program space memory.

The DM_PG[4..0] bits are used as Page address bits for Data memory accesses. The DSP's address A0-A14 plus the 5 DM_PG[4-0] are combined to make a 19 bit word address. Both the SRAM and the FLASH as well as the Daughter Card Interface use this access mechanism.

> (Note that the SRAM pages are 32K each, and the FLASH pages are 32K each.) With the five DM_PG bits provided, thirty-two, 32K data memory pages can be accessed onboard, as well as on a daughter card.

The table below shows the DM_CTL bit definitions.

Table 6: Data Memory (DM_CNTL) Bit Definitions

Bit #	Name	R/W	Description
7	DM_SEL	R/W	Data Memory Selection (**0=on board memory**, 1 daughter card)
6	MEMTYPE_DS	R/W	**0= FLASH ENABLED**, 1 = SRAM Memory For Data Space Access
5	MEMTYPE_PS	R	**0= FLASH ENABLED**, 1 = SRAM Memory For Program Space Access
4	DM_PG4	R/W	Flash/SRAM/Daughter Cards Memory Page Bit 4 **(defaults to 0)** MSB
3	DM_PG3	R/W	Flash/SRAM/Daughter Cards Memory Page Bit 3 **(defaults to 0)**
2	DM_PG2	R/W	Flash/SRAM/Daughter Cards Memory Page Bit 2 **(defaults to 0)**
1	DM_PG1	R/W	Flash/SRAM/Daughter Cards Memory Page Bit 1 **(defaults to 0)**
0	DM_PG0	R/W	Flash/SRAM/Daughter Cards Memory Page Bit 0 **(defaults to 0)** LSB

Descriptions appearing in **bold** are defaults.

2.2.4.1.6 MISC Register (I/O Address 0x0006)

The MISC Register contains function bits that control data memory access width, the DSP's MCBSP2 selection and the Codec Control Shift register ready status.

DB_WIDE determines whether daughter card data memory and I/O accesses are 16 or 32-bit. When 32-bit (wide) mode is selected, daughter card data memory and I/O accesses are asserted to the daughter card based on the DB_32ODD selection. When DB_WIDE is 0, 16-bit accesses are performed, and when DB_WIDE is 1, 32-bit accesses are performed.

DB_32ODD selects whether a 32 bit daughter card accesses are to an even (0) or odd (1) address. This selection is required to enable data and I/O selects to the daughter card at the appropriate time. If a 32-bit daughter card access is to an odd address, then DB_32ODD should be to 1. If a 32-bit daughter card access is to an even address, then DB_32ODD should be 0. For, 32-bit daughter card writes, the upper 16 bits should be written first to the destination address plus 1, and then lower 16 bits should be written to the destination address. For example, for a 32-bit write to daughter card memory at 0x8000, DB_32ODD should be 0, the most-significant word (MSW) should be written to 0x8001, and the least-significant word (LSW) should be written to 0x8000. For 32-bit daughter card reads, the lower 16 bits should be read first from the source address, and then the upper 16 bits should be read from the source address plus 1. For example, for a 32-bit read from daughter card memory at 0x8001, DB_32ODD should be 1, the LSW should be read from 0x8001 and the MSW should be read from 0x8002

CODEC_RDY is the status bit of the Control channel shift register for the on board PCM3002 Codec. Before writing to the Codec Control channel the CODEC_RDY bit should be checked.

BSP2SEL is used to determine if the McBSP 2 channel on the 5416 is used to access the data channel on the onboard PCM3002 codec or if the McBSP 2 channel will be routed to the HPI Expansion Connector.

Table 7: MISC Register Bit Definitions

Bit #	Name	R/W	Description
7	CODEC Ready	R	CODEC Command Transfer Ready (0-ready, 1=not ready)
6	0	R	Always zero
5	0	R	Always zero
4	0	R	Always zero
3	0	R	Always zero
2	DC_WIDE	R/W	Daughter Card Data Memory Width Select (**0=16 bits**, 1=32 bits)
1	DC32_ODD	R/W	32 Bit Daughter Card Address Access Mode (**0=even**, 1=odd)
0	BSP2SEL	R/W	McBSP2 Select (**0=PCM3002 Data Channel**,1=Daughter card)

2.2.4.1.7 CODEC_CLK Register (I/O Address: 0x0007)

This register controls the divide ratio of the PCM3002 Codec. At reset the register is initialized to zero (0x00). The Codec input Clock is 12.288 Megahertz at reset. The Codec Output clock is equal to the Codec input Clock resulting in a 48Khertz sample rate. The Codec input clock can be divided and sent to the codec output Clock via this register. The CLK_DIV bits are only valid when the DIV_SEL bit is set to 1.

Table 8: Codec Clock Register Bit Definitions

Bit #	Name	R/W	Description
7	0	R	Always zero
6	0	R	Always zero
5	0	R	Always zero
4	0	R	Always zero
3	DIV_SEL	R/W	1=Codec Clock Divide Selected Rate is set by CLK_DIV Bits 0=Codec In Clock same as Codec Out Clock
2	CLK_STOP	R/W	CLK_STOP
1	CLK_DIV1	R/W	00 divide by 2 (fs=24Khz.), 01=divide by 4 (fs=12Khz), 10=divide by 6 (fs=8Khz), 11 divide by 8 (fs=6Khz)
0	CLK_DIV0	R/W	

There is a specific sequence that must be followed when changing the Clock divider to ensure proper operation. This sequence is outlined below.

1) Set the CLK_STOP bit
   CODEC_CLK_REG = CODEC_CLK_REG | CLK_STOP;

2) Set the CLK_DIV1 and CLK_DIV0 bits
   CODEC_CLK_REG = (CODEC_CLK_REG & ~0x03) | (USER_CLK_DIV1 |
   USER_CLK_DIV0);

3) Reset the CLK_STOP bit
   CODEC_CLK_REG = CODEC_CLK_REG & ~CLK_STOP;

4) Set the DIV_SEL
   CODEC_CLK_REG = CODEC_CLK_REG | DIV_SEL;

2.2.5 Flash ROM Interface

The 256K word Flash is mapped into the VC5416's program space and data space. This flash is meant for boot loading of programs using the VC5416's parallel boot loader in microcontroller mode or direct loading in microprocessor mode.

For data space accesses there are eight pages (8) of 32K words of flash mapped in the VC5416's data space from 0x8000 to 0xFFFF. The selected page is determined by the CPLD's DM_PG[4:0] bits in the DM_CTRL register. These pages are referred to as F_PAGE0 - F_PAGE7 for easy reference. Various control bits in the DM_CTRL register and the VC5416's internal PMST register affect the decoding as shown in the tables below.

The table below shows how this memory is mapped via data memory accesses. External Data Accesses in 0x08000-0x0FFFF are paged with A0-A14 being supplied directly by the DSP and page address DM_PG[0-4] being supplied by the interface CPLD.

Note: Address line A15 is not used but must be a '**1**' to access external data space.

Table 9: FLASH ROM Data Space Access Addressing

				A15=1	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DSP Address
DM_PG4	DM_PG3	DM_PG2	DM_PG1	DM_PG0																Page Address
M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Memory Address

A[15:0] is DSP Address
DM_PG[4:0] are located in DM_CTNL Register of CPLD at I/O Location 0x0005 bits 4-0. See section 2.2.4.1.5 that discusses the DM_CTNL register.
M[19:0] is memory Address

The PMST Register and the interface CPLD are the factors that control the Data memory decoding as shown in the table below.

Table 10: Flash ROM Data Memory Address

DSP ADDRESS RANGE	DM_PG[4.0]**	DROM*	DM_SEL**	MEMTYPE_DS**	ACCESS
0x0000-0x07FFF	X	X	X	X	Internal DARAM and Registers
0x8000-0xFFFF	X	1	X	X	Internal DARAM
0x8000-0xFFFF	0	0	0	0	External (F_PAGE0)
0x8000-0xFFFF	1	0	0	0	External (F_PAGE1)
0x8000-0xFFFF	2	0	0	0	External (F_PAGE2)
0x8000-0xFFFF	3	0	0	0	External (F_PAGE3)
0x8000-0xFFFF	4	0	0	0	External (F_PAGE4)
0x8000-0xFFFF	5	0	0	0	External (F_PAGE5)
0x8000-0xFFFF	6	0	0	0	External (F_PAGE6)
0x8000-0xFFFF	7	0	0	0	External (F_PAGE7)
0x8000-0xFFFF	8-31	0	0	0	External Flash IMAGES

Note: External address is A0-A14 plus 5 page register bits.
* in VC5416 processor's PMST register
** in CPLD registers

Program space directly accesses the flash memory as long as the access is between 0x000000 to 0x3FFFFF. The overlay and MP/MC- bits in the PMST register will determine if the memory is internal or external. MEMTYPE_PS determines if SRAM or flash ROM is selected.

Table 11: Flash ROM Program Memory Address

DSP ADDRESS RANGE	MP/$\overline{MC}$ *	OVLY *	MEMTYPE_PS**	ACCESS
0x000000-0x007FFF	X	1	X	Internal
0x000000-0x007FFF	X	0	0	External F_PAGE 0
0x008000-0x00BFFF	X	X	0	External F_PAGE 1
0x00C000-0x00FFFF	0	X	X	Internal
0x00C000-0x00FFFF	1	X	0	External F_PAGE 1
0x01000-0x017FFF	X	1	0	Internal
0x010000-0x017FFF	X	0	X	External F_PAGE 2
0x018000-0x01FFFF	X	X	0	External F_PAGE 3
0x020000-0x027FFF	X	1	X	Internal
0x020000-0x027FFF	X	0	0	External F_PAGE 4
0x028000-0x02FFFF	X	X	0	External F_PAGE 5
0x030000-0x037FFF	X	1	X	Internal
0x030000-0x037FFF	X	0	0	External F_PAGE 6
0x038000-0x03FFFF	X	X	0	External F_PAGE 7
		. . .	***IMAGES***	
0x3F8000-0x3FFFFF	X	1	X	External Image F_PAGE 7
0x400000-0x407FFF	X	1	0	Internal
0x408000-0x40FFFF	X	X	0	Daughter Card Access in 32K pages (0x8000-0xFFFF) if OVLY=1 All pages from 0x400000-0x7FFFFF if OVLY=0

* in VC5416 processor
** in CPLD

2.2.6 SRAM Interface

The 64K word SRAM is mapped into the VC5416's program space and data space. This SRAM provides a mechanism to support on chip DMA and allows development of boot code for flash rom

For data space accesses there are two pages (2) of 32K words of SRAM mapped in the VC5416's data space from 0x8000 to 0xFFFF. The selected page is determined by the CPLD's DM_PG[4:0] bits in the DM_CTRL register. These pages are referred to as SR_PAGE0 and SR_PAGE1 for easy reference. Various control bits in the DM_CTRL register and the VC5416's internal PMST register affect the decoding as shown in the tables below.

The table below shows how this memory is mapped via data memory accesses. External Data Accesses in 0x08000-0x0FFFF are paged with A0-A14 being supplied directly by the DSP and page address DM_PG[0-4] being supplied by the interface CPLD.

Note: Address line A15 is not used but must be a '**1**' to access external data space.

Table 12: SRAM Data Space Access Addressing

				A15=1	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DSP Address
DM_PG4	DM_PG3	DM_PG2	DM_PG1	DM_PG0																Page Address
M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Memory Address

A[15:0] is DSP Address
DM_PG[4:0] are located in DM_CTNL Register of CPLD at I/O Location 0x0005 bits 4-0. See section 2.2.4.1.5 that discusses the DM_CTNL register.
M[19:0] is memory Address

The PMST Register and the interface CPLD are the factors that control the Data memory decoding as shown in the table below.

Table 13: SRAM Data Memory Address

DSP ADDRESS RANGE	DM_PG[4.0]**	DROM*	DM_SEL**	MEMTYPE_DS**	ACCESS
0x0000-0x07FFF	X	X	X	X	Internal DARAM and Registers
0x8000-0xFFFF	X	1	X	X	Internal DARAM
0x8000-0xFFFF	0	0	0	1	External (SR_PAGE0)
0x8000-0xFFFF	1	0	0	1	External (SR_PAGE1)
0x8000-0xFFFF	2-31	0	0	1	External SRAM IMAGES

Note: External address is A0-A14 plus 5 page register bits.
* in VC5416 processor's PMST register
** in CPLD registers

Program space directly accesses the SRAM as long as the access is between 0x000000 to 0x3FFFFF. The overlay and MP/MC- bits in the PMST register will determine if the memory is internal or external. MEMTYPE_PS determines if SRAM or flash ROM is selected.

Table 14: SRAM Program Memory Address

DSP ADDRESS RANGE	MP/$\overline{MC}$ *	OVLY *	MEMTYPE_PS**	ACCESS
0x000000-0x007FFF	X	1	X	Internal
0x000000-0x007FFF	X	0	1	External SR_PAGE 0
0x008000-0x00BFFF	X	X	1	External SR_PAGE 1
0x00C000-0x00FFFF	0	X	X	Internal
0x00C000-0x00FFFF	1	X	1	External SR_PAGE 1
0x01000-0x017FFF	X	1	0	Internal
0x010000-0x017FFF	X	0	X	Image SR_PAGE 0
0x018000-0x01FFFF	X	X	0	Image SR_PAGE 1
		. . .	***IMAGES***	
0x3F8000-0x3FFFFF	X	1	X	Image SR_PAGE 1
0x400000-0x407FFF	X	1	0	Internal
0x408000-0x40FFFF	X	X	0	Daughter Card Accesses in 32K pages (0x8000-0xFFFF) if OVLY=1 All pages from 0x400000-0x7FFFFF if OVLY=0

* in VC5416 processor
** in CPLD

2.2.7 Codec Interface

The DSK uses a PCM3002 stereo Codec to provide analog inputs and outputs. The interface to the codec is through two channels, one for control the other for data. The CPLD on the DSK's is used to interface to the control channel via 2 –8 bit registers in I/O space CODEC_L and CODEC_H. Furthermore, the CPLD generates all required timing signals for the PCM3002 via a clock oscillator and the CODEC_CLK control register. The default CODEC system clock is 12.488-MHz. The CPLD uses the CODEC system clock to generate a bit clock of 3.0122-MHz and a frame sync signal of 48-KHz. This can be changed to other frequencies as outlined in the CODEC_CLK section of the CPLD. The Data to the codec, is supplied via the VC5416's McBSP2 interface. There is a bit in the MISC register of the CPLD which will allow the McBSP2 register to be routed to the HPI expansion connector, however, the default path is to the PCM3002 Codec.

The diagram below shows the interconnection between the Codec, CPLD, and DSP.

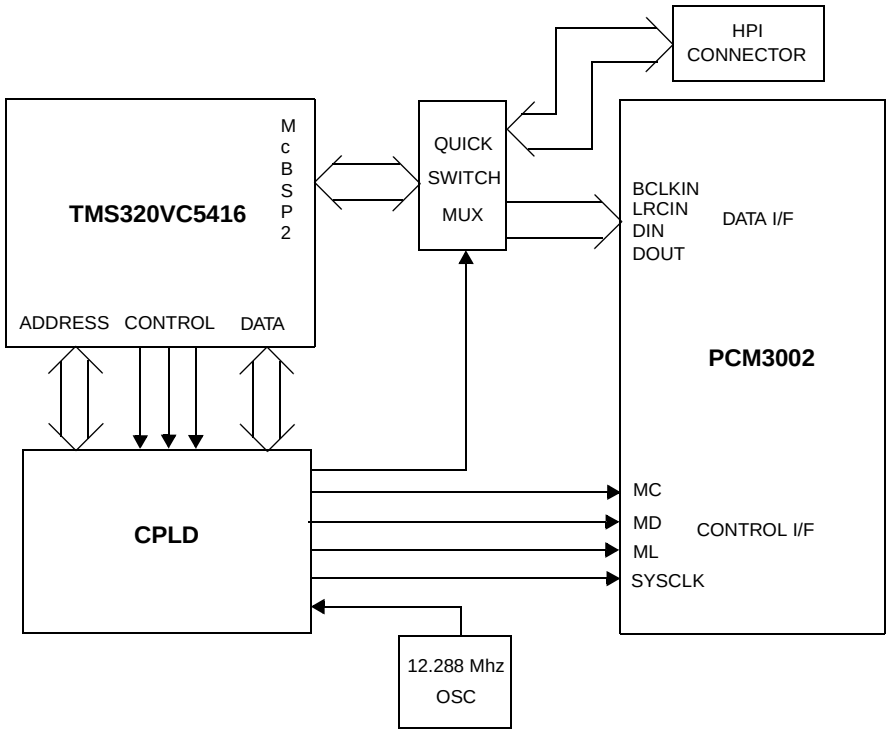


Figure 2-6, TMS320VC5416 DSK CODEC INTERFACE

2.2.7.1 Programming the Codec Control Interface

The PCM3002 Control Interface has four 16-bit internal registers that are software controlled via a serial interface. The CPLD has two internal 8-bit registers that when written in sequence will transfer their contents to the CODEC's control interface. The serial master control signals of the CODEC consist of the CODEC_MC (master clock), CODEC_MD (master data), and CODEC_ML (master load).

To write a control word to the CODEC, the user will write two 8-bit bytes to the CPLD at I/O locations 0x0002 (CODEC_L), and 0x0003 (CODEC_H). The first byte is the lower order byte of the 16-bit control word, the second byte is the higher order byte of the 16-bit control word.

After the completion of the write to CODEC_H, the CPLD will automatically transmit the data serially to the CODEC control interface over the master control signals. Before another Control Interface Codec Transfer is done, the programmer needs to check the CODEC_RDY bit in the MISC Register of the CPLD (IO address 0x0006 bit 7). This bit gives the current state of the control interface shift register in the CPLD.

For additional information about the control bits of the CODEC, please refer to the PCM3002 data sheet.

2.2.7.2 Programming the Data interface

The Data interface on the PCM3002 is connected to the McBSP2 pins on the VC5416 DSP. The table below shows the pin assignments of this interconnection.

Table 15: PCM3002 - VC5416 Interconnect

PCM3002		CPLD		VC5416	
Signal	**Type**	**Signal**	**Type**	**Signal**	**Type**
SYSCLK	I	CODEC_CLK	O	N/A	
BCLKIN	I	CODEC_BCLK	O	BCLKR2 BCLKX2	I
LRCIN	I	N/A		BFSR2 BFSX2	O
DIN	I	N/A		BDX2	O
DOUT	O	N/A		BDR2	I

The CPLD has a CODEC_CLK register that allows the programmer to change the sampling frequencies shown in the CODEC_CLK register section.

2.2.7.3 PCM3002 Codec Input/Output Circuitry

Four industry standard 3.5 mm. connectors are used in the audio interface, one for line-level audio inputs, one for a microphone, one for line-level audio outputs, and one for speakers or headphones. The line-level inputs are stereo, while the microphone input only supports a single channel (mono). On the output side there are stereo connections on both the amplified and unamplified signals.

The two analog inputs (line and microphone) are AC coupled, active filtered and mixed prior to being digitized by the PCM3002E connected to the McBSP2 port of the DSP. The line-level input has a fixed gain of 0dB. The line-level inputs support signal levels of up to 2Vrms. The microphone input is designed for electret microphones that require a bias voltage. A dynamic microphone can be used if capacitors are used to block the bias voltage. The maximum allowable signal level from the microphone is 1 Vrms. The microphone input has a potentiometer which allow the user to adjust gain on the microphone input.

The DAC output from the PCM3002 CODEC has programmable attenuation from +0dB to mute in –1.5dB increments. The DAC output channel is filtered using a multiple-feedback 2^{nd} order active filter. The post-filter has a cut-off frequency of 30KHz. The post-filtered information is directly passed to a standard stereo audio jack for line-level loads (~10Kohms) and also passed through an output driver stage for connection to low impedance speakers or headphones (e.g. 8 to 32 ohms).

2.2.8 Daughter Card Memory Interface

The 5416 DSK supports the standard daughter card interface interconnections. Accesses to the Daughter-cards can be done via Program Space, Data Space, or I/O space. On the 5416 DSK Daughter cards all spaces support 16 data bits transfers and Data Space and I/O accesses can support 32 data bits transfers. DM_SEL must be set for data space accesses. I/O space and program space accesses use memory decode to control accesses

It is recommended to run the EMIF in CLKOUT/2 mode at higher clock rates (above 100 MHz) to avoid buffer conflicts.

Sample programs for accessing daughter card 16 bit program memory, 16 and 32 bit data memory, and 16 and 32 bit I/O memory are included in the .pdf file: c:\TI\docs\pdf\5416_dsk_expsw.pdf.

2.2.8.1 Program Space Accesses

Daughter-Card Program Space accesses on the DSK are available when A22 is a logic 1. All Daughter Card Program Space accesses are 16 bits wide. Therefore, all external accesses from 0x400000 to 0x7FFFFF access the daughter card space. Note that if the OVLY bit is selected only the upper 32K of each (0x8000 - 0xFFFF) is mapped to the daughter card interface. These accesses are shown in the table below:

Table 16: Program Space Accesses

DSP Address Range	OVLY *	Access
0x000000-0x3FFFFF	X	On-board/internal
0x400000-0x407FFF	1	Internal DSP Access
0x400000-0x407FFF	0	Daughtercard
0x408000-0x40FFFF	X	Daughtercard
0x410000-0x417FFF	1	Internal DSP Access
0x410000-0x417FFF	0	Daughtercard
0x418000-0x41FFFF	X	Daughtercard
0x42000 to 0x7FFFF	See above maps	Same as above maps

* In VC5416 processor

2.2.8.2 Data Space Accesses

Daughter card data memory accesses on the DSK are available when A15 is a logic 1, DROM is turned off in the PMST register, and the DM_SEL bit in the DM_CNTL register of the CPLD is set to 1. The address range from the DSP is 0x8000 to 0xFFFF, however the 5 DM_PG[0:4] bits are added to the DSP's A0-A14 lines to make thirty-two (32) 32K 16 bit accessible pages.

Both 16 and 32 bit accesses are available for the data space accesses. These accesses are shown in the table below:

Table 17: Data Space Accesses

DSP Address Range	DM_PG[4:0]**	DROM*	DM_SEL**	MEMTYPE_DS**	DC_WIDE**	DC32_ODD**	ACCESS
0x0000-0x7FFF	X	X	X	X	X	X	Internal
0x8000-0xFFFF	X	X	0	X	X	X	Onboard/internal
0x8000-0xFFFF	0	0	1	X	0	X	Daughtercard 16 bit access page 0
0x8000-0xFFFF	1:31	0	1	X	0	X	Daughtercard 16 bit access page 1-31
0x8000-0xFFFF	0	0	1	X	1	0	Daughtercard 32 bit access page 0 even address
0x8000-0xFFFF	0	0	1	X	1	1	Daughtercard 32 bit access page 0 odd address
0x8000-0xFFFF	1:31	0	1	X	1	0	Daughtercard 32 bit access page 1-31 even address
0x800-0x7FFFF	1:31	0	1	X	1	1	Daughtercard 32 bit access page 1-31 odd address

2.2.8.2.1 Data Space 32 Bit Accesses

Like with 16 bit data accesses there are two 32 (thirty-two) 32K word pages available to daughter card accesses. However, for 32 bit data space accesses specific sequences must be programmed to get correct 32 bit wide data transfers

For even address sequences (e.g. 0x28400) the accesses are broken up into 2 accesses one at 0x8400 and one at 0x8401.Note the upper address comes from the DM[0:4] bits. The DC-32 Odd bit in the CPLD MISC register should be set to 0, and the sequence below shows the correct access procedure.

Write Sequence:

1. Set the page address in DM_CTNL to 00101 binary. This will point to page 0x28.
2. Set the DC_WIDE bit and clear the DC32_ODD bit in the CPLD MISC register
3. Do the 2 Data Space accesses:
    - Most Significant WORD at ODD address (0x8401)
    - Least Significant word at EVEN address (0x8400)
4. Turn off the DC_WIDE bit in the MISC register

Read Sequence

1. Set the page address in DM_CTNL to 00101 binary. This will point to page 0x28.
2. Set the DC_WIDE bit and clear the DC32_ODD in the CPLD MISC register
3. Do the 2 Data Space accesses:
    - Least Significant WORD at EVEN address (0X8400)
    - Most Significant word at ODD address (0x8401)
4. Turn off the DC_WIDE bit in the MISC register

For Odd address sequences (e.g. 0x28401) the accesses are broken up into 2 accesses one at 0x8401 and one at 0x8402. The DC-32 Odd bit in the CPLD MISC register should be set to 1, and the sequence below shows the correct access procedure

Write Sequence:

1. Set the page address in DM_CTNL to 00101 binary. This will point to page 0x28.
2. Set the DC_WIDE bit and clear the DC32_ODD in the CPLD MISC register
3. Do the 2 Data Space accesses:
    - Most Significant WORD at EVEN address (0x8402)
    - Least Significant word at ODD address (0x8401)
4. Turn off the DC_WIDE bit in the MISC register

Read Sequence

1. Set the page address in DM_CTNL to 00101 binary. This will point to page 0x28.
2. Set the DC_WIDE bit and clear the DC32_ODD in the CPLD MISC register
3. Do the 2 Data Space accesses:
    - Least Significant WORD at EVEN address (0x8401)
    - Most Significant word at ODD address (0x8402)
4. Turn off the DC_WIDE bit in the MISC register

2.2.8.3 I/O Space Accesses

Daughter-Card I/O Space accesses on the DSK are available when the DSP's address bit A15 is a logic 1. The address range for I/O accesses is 32K Words from 0x8000 to 0xffff. Access data width can be either 16 bits or 32 bits wide. These accesses are shown in the table below:

Table 18: I/O Space Accesses

DSP Address Range	DC_WIDE **	DC32_ODD**	Access
0x0000-0x7FFF	X	X	On-board
0x8000-0xFFFF	0	X	Daughtercard 16 bit Access
0x8000-0xFFFF	1	0	Daughtercard 32 bit Access
0x8000-0xFFFF	1	1	Daughtercard 32 bit Access

** In CPLD

Note specific sequences are necessary for 32 bit access. For 16 bit accesses there is no specific programming sequences that need to be implemented.

2.2.8.3.1 I/O Space 32 Bit Accesses

For 32 bit accesses specific sequences must be programmed to get correct 32 bit wide data transfers

For even address sequences (e.g. 0xC000) the accesses are broken up into 2 accesses one at 0xC000 and one at 0xC001. The DC-32 Odd bit in the CPLD MISC register should be set to 0, and the sequence below shows the correct access procedure.

Write Sequence:

1. Set the DC_WIDE bit and clear the DG32_ODD bit in the CPLD MISC register
2. Do the 2 I/O accesses:
    - Most Significant WORD at ODD address (0xC001)
    - Least Significant word at EVEN address (0xC000)
3. Turn off the DC_WIDE bit in the MISC register

Read Sequence

1. Set the DC_WIDE bit and clear the DG32_ODD bit in the CPLD MISC register
2. Do the 2 I/O accesses:
    - Least Significant WORD at EVEN address (0XC000)
    - Most Significant word at ODD address (0xC001)
3. Turn off the DC_WIDE bit in the MISC register

For Odd address sequences (e.g. 0xC001) the accesses are broken up into 2 accesses one at 0xc001 and one at 0xc0002. The DC-32 Odd bit in the CPLD MISC register should be set to 1, and the sequence below shows the correct access procedure

Write Sequence:

1. Set the DC_WIDE and DC32_ODD bits in the CPLD MISC register
2. Do the 2 I/O accesses:
    - Most Significant WORD at EVEN address (0xC002)
    - Least Significant word at ODD address (0xC001)
3. Turn off the DC_WIDE bit in the MISC register

Read Sequence

1. Set the DC_WIDE and DC32_ODD bits in the CPLD MISC register
2. Do the 2 I/O accesses:
    - Least Significant WORD at EVEN address (0xC001)
    - Most Significant word at ODD address (0xC002)
3. Turn off the DC_WIDE bit in the MISC register

2.2.9 Wait States

The TMS320VC5416 has an on chip wait state generator controller controlled by registers SWWSR and SWCR mapped in the data memory. The table below shows these 2 registers and their function.

2.2.9.1 Software Wait State Generator

The software wait state generator on the TMS320VC5416 can be extended external bus cycles by up to 14 machine cycles. Devices that require more then 14 wait-states can be interfaced using the hardware READY line.

The software wait state register, SWWSR, controls the operation of the wait state generator. The 14 LSBs of the SWWSR specifies the number of wait states (0-7) to be inserted for external memory accesses to five separate ranges. This allows a different number of wait states for each of the 5 address ranges. Additionally, the software wait state multiplier, SWSM, bit of the wait state control register, SWCR, defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait state generator is initialized to provide 7 wait states on all external memory accesses. The SWWSR bit fields are shown in the table below.

Table 19: SWWSR Register Bit Fields

Bits	15	14 12	11 9	8 6	5 3	2 0
Space	XPA	I/O	Data	Data	Program	Program
Read, Write	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	111	111	111	111	111

The bit fields in SWWSR are described in the table below.

Table 20: SWWSR Bit Field Definition

Bit #	Bit Name	Reset Value	Function
15	XPA	0	Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0-5) to select the address range for program space wait states
14-12	I/O	111	I/O space. The field value (0-7) corresponds to the base number of wait states for I/O space accesses within addresses 0x0000-0xFFFF. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
11-9	Data	111	Upper Data Space. The field value (0-7) corresponds to the base number of wait states for external data space accesses within addresses 0x8000-0xFFFF. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
8-6	Data	111	Lower Data Space. The field value (0-7) corresponds to the base number of wait states for external data space accesses within addresses 0x0000-0x7FFF. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
5-3	Program	111	Upper Program Space. The field value (0-7) corresponds to the base number of wait states for external program space accesses within addresses: - XPA= 0: 0x8000 - 0xFFFF - XPA= 1: The upper program space bit field has no effect on wait states The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2-0	Program	111	Lower Program Space. The field value (0-7) corresponds to the base number of wait states for external program space accesses within addresses: - XPA= 0: 0x8000 - 0x7FFF - XPA= 1: 0x00000 - 0xFFFFF The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.

The software wait state multiplier bit of the software wait state control register, SWWSR, is used to extend the base number of wait states selected by the SWWSR. The SWSR bit fields are shown in the table below.

Table 21: Software Wait State Control Register Bits Fields

Bit #	15 1	0
Function	Reserved	SWSM
Reset, Write	R/W	R/W
Reset Value	0	0

The bit fields in SWWSR are described in the table below.

Table 22: SWWSR Bit Field Definition

Bit #	Bit Name	Reset Value	Function
15-1	Reserved	0	These bits are reserved and unaffected by writes
0	SWSM	0	Software wait state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. - SWSM = 0: wait state base values are unchanged (multiplied by 1) - SWSM = 1: wait state base values are multiplied by 2 for a maximum of 14 wait states.

This controller allows various regions in memory to be programmed to different wait state values. The TMS320VC5416 powers up with maximum wait states. On the TMS320VC5416 DSK the access time for various components in the table below.

Table 23: Memory Wait States

Device	Access Time	Decoder	Total Access Time
SRAM	12 ns.	10 ns.	22 ns.
Flash	70 ns.	10 ns.	80 ns.
CPLD	60 ns.		60 ns.

The access time on the TMS320VC5416 is t_a(A)M1 for non-consecutive accesses and t_a(A)M2 for consecutive accesses. The table below shows various access times for various frequencies.

Table 24: Access Times

Frequency	2H	Each Wait State	t_a(A)1st Cycle (2H-4)
160 Mhz.	6.25 ns.	WS*6.25 ns.	2.25 ns.
120 Mhz.	8.33 ns.	WS*8.33 ns.	6.4 ns.
96 Mhz.	10.4 ns.	WS*10.4 ns.	6.4 ns.
48 Mhz.	20.83 ns.	WS*20.83 ns.	16.83 ns.

It is recommended to operate the EMIF in CLKOUT/2 mode at higher frequencies (CPU frequency from 96 - 160 Mhz.) to avoid buffer contention from daughter card buffers. Note that wait states with EMIF in CLKOUT/2 mode can be programmed to one-half the value in the table below.

The table below shows the maximum wait states for the various frequencies. various frequencies.

Table 25: Minimum Wait States

Frequency	SRAM	Flash	CPLD
160 Mhz.	3	12	9
120 Mhz.	2	10	7
96 Mhz.	2	7	6
48 Mhz.	0	4	3

2.3 TMS320VC5416 DSK Jumpers

The TMS320VC5416 DSK has a single jumper block, JP4, which controls the power up CLKMODE and MP/MC setting.

2.3.1 JP4, DSP Clock and Mode Configuration

Jumper JP4 is a 4 x 2 connector that determines the power up CLKMODE on the DSP, and selects whether the DSP is in microcomputer mode or microcontroller mode. The table below shows the clock and mode selection settings.

Table 26: JP4, DSP Configuration

CLKMD1	CLKMD2	CLKMD3	MP/MC	Clock Mode	DSP MP/MC Mode
OFF	OFF	OFF	OFF	1/2 x CLKIN PLL Off, OSC On	Microprocessor Mode
OFF	OFF	ON	OFF	1 x CLKIN PLL On, OSC On	Microprocessor Mode
OFF	ON	OFF	OFF	1/4 x CLKIN PLL Off, OSC On	Microprocessor Mode
OFF	ON	ON	OFF	2 x CLKIN PLL On, OSC On	Microprocessor Mode
ON	OFF	OFF	OFF	RESERVED	Microprocessor Mode
ON	OFF	ON	OFF	5 x CLKIN PLL On, OSC On	Microprocessor Mode
ON	ON	OFF	OFF	10 x CLKIN PLL On, OSC On	Microprocessor Mode
ON	ON	ON	OFF	1/2 x CLKIN PLL Off, OSC Off	Microprocessor Mode
OFF	OFF	OFF	ON	1/2 x CLKIN PLL Off, OSC On	Microcontroller Mode
OFF	OFF	ON	ON	1 x CLKIN PLL On, OSC On	Microcontroller Mode
OFF	ON	OFF	ON	1/4 x CLKIN PLL Off, OSC On	Microcontroller Mode
OFF	ON	ON	ON	2 x CLKIN PLL On, OSC On *****	Microcontroller Mode
ON	OFF	OFF	ON	RESERVED	Microcontroller Mode
ON	OFF	ON	ON	5 x CLKIN PLL On, OSC On	Microcontroller Mode
ON	ON	OFF	ON	10 x CLKIN PLL On, OSC On	Microcontroller Mode
ON	ON	ON	ON	1/2 x CLKIN PLL Off, OSC Off	Microcontroller Mode

Note: "*****" is the default setting. This is the 2 x CLKIN PLL On, OSC On, Microcontroller Mode

The figure below show JP4 in the default configuration.

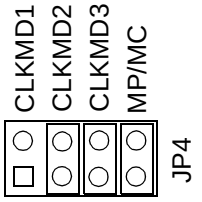


Figure 2-7, JP4, DSP Configuration - Default Setting

2.4 TMS320VC5416 DSK Connectors

The TMS320VC5416 DSK has sixteen (16) connectors which provide the user access to the various on the DSK. The position of each connector is identified in Figure 2-1.These connectors, their size, their function, and the side of the printed circuit board they are mounted on are shown in the table below.

Table 27: TMS320VC5416 DSK Connectors

Connector	# Pins	Function
P1	80	Memory
P2	80	Peripheral
P3	80	HPI
J1	2	Microphone
J2	2	Line In
J3	2	Line Out
J4	2	Speaker
J5 *****	4	Optional Power Connector
J6	2	+5 Volt
J7	14	External JTAG
J201	5	USB JTAG
JP1	10	CPLD Programming
JP4	8	DSP Configuration Jumper

Note: "*****" Not populated

2.4.1 Expansion Connectors

The TMS320VC5416 DSK supports three expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following three sections.

Note: I is on an Input pin
O is on an Output pin
Z is on a High Impedance pin

2.4.2 P1, Memory Expansion Connector

Table 28: P1, Memory Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+5 Volts	O	2	+5 volts	O
3	DC_A19	O	4	DC_A18	O
5	DC_A17	O	6	DC_A16	O
7	DC_A15	O	8	DC_A14	O
9	DC_A13	O	10	DC_A12	O
11	GND	O	12	GND	O
13	DC_A11	O	14	DC_A10	O
15	DC_A9	O	16	DC_A8	O
17	DC_A7	O	18	DC_A6	O
19	DC_A5	O	20	DC_A4	O
21	+5 Volts	O	22	+5 Volts	O
23	DC_A3	O	24	DC_A2	O
25	DC_A1	O	26	DC_A0	O
27	DC_A21	O	28	DC_A20	O
29	GND	O	30	GND	O
31	GND	O	32	GND	O
33	DC_D31	I/O/Z	34	DC_D30	I/O/Z
35	DC_D29	I/O/Z	36	DC_D28	I/O/Z
37	DC_D27	I/O/Z	38	DC_D26	I/O/Z
39	DC_D25	I/O/Z	40	DC_D24	I/O/Z
41	+3.3 Volts	O	42	+3.3 Volts	O
43	DC_D23	I/O/Z	44	DC_D22	I/O/Z
45	DC_D21	I/O/Z	46	DC_D20	I/O/Z
47	DC_D19	I/O/Z	48	DC_D18	I/O/Z
49	DC_D17	I/O/Z	50	DC_D16	I/O/Z
51	GND	O	52	GND	O
53	DC_D15	I/O/Z	54	DC_D14	I/O/Z
55	DC_D13	I/O/Z	56	DC_D12	I/O/Z
57	DC_D11	I/O/Z	58	DC_D10	I/O/Z
59	DC_D9	I/O/Z	60	DC_D8	I/O/Z
61	GND	O	62	GND	O
63	DC_D7	I/O/Z	64	DC_D6	I/O/Z
65	DC_D5	I/O/Z	66	DC_D4	I/O/Z
67	DC_D3	I/O/Z	68	DC_D2	I/O/Z
69	DC_D1	O	70	DC_D0	O
71	GND	O	72	GND	O
73	DC_RE-	O	74	DC_WE-	O
75	DC_OE-	O	76	DC_RDY	I
77	DC_MSTRB-	O	78	DC_DS-	O
79	GND	O	80	GND	O

2.4.3 P2, Peripheral Expansion Connector

Table 29: P2, Peripheral Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+12 Volts *	O	2	-12 Volts *	O
3	GND	O	4	GND	O
5	+5 Volts	O	6	+5 Volts	O
7	GND	O	8	GND	O
9	+5 Volts	O	10	+5 Volts	O
11	RESERVED		12	RESERVED	
13	RESERVED		14	RESERVED	
15	RESERVED		16	RESERVED	
17	RESERVED		18	RESERVED	
19	+3.3 Volts	O	20	+3.3 Volts	O
21	DC_BCLKX0	I/O/Z	22	RESERVED	
23	DC_BFSX0	I/O/Z	24	DC_BDX0	O/Z
25	GND	O	26	GND	O
27	DC_BCLKR0	I/O/Z	28	RESERVED	
29	DC_BFSR0	I/O/Z	30	DC_BDR0	I
31	GND	O	32	GND	O
33	DC_BCLKX1	I/O/Z	34	RESERVED	
35	DC_BFSX1	I/O/Z	36	DC_BDX1	O/Z
37	GND	O	38	GND	O
39	DC_BCLKR1	I/O/Z	40	RESERVED	
41	DC_BFSR1	I/O/Z	42	DC_BDR1	Z
43	GND	O	44	GND	O
45	DC_TOUT	O	46	RESERVED	
47	RESERVED		48	DC_INT1-	I
49	DC_XF	O	50	DC_BIO-	I
51	GND	O	52	GND	O
53	INT3-	I	54	RESERVED	
55	RESERVED		56	DC_IOSTRB-	O
57	RESERVED		58	RESERVED	
59	RESET-	O	60	RESERVED	
61	GND	O	62	GND	O
63	DC_CNTL1	O	64	DC_CNTL0	O
65	DC_STAT1	I	66	DC_STAT0	I
67	DC_INT2-	I	68	DC_INT3-	I
69	DC_PS-	O	70	DC_IS-	O
71	RESERVED		72	RESERVED	
73	RESERVED		74	RESERVED	
75	DC_DETECT-	I	76	GND	O
77	GND	O	78	DC_CLKOUT/2	O
79	GND	O	80	GND	O

* Provided from optional power connector J5

2.4.4 P3, HPI Expansion Connector

Table 30: P3, HPI Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+5 Volts	O	2	+5 Volts	O
3	HP_BCLKX2	I/O/Z	4	HP_BCLKR2	I/O/Z
5	HP_BFSX2	I/O/Z	6	HP_BFSR2	I/O/Z
7	HP_BDX2	O/Z	8	HP_BDR2	I
9	RESERVED		10	HP_CLKOUT/2	O
11	GND	O	12	GND	O
13	HP_HRW	I	14	HP_HCNTL0	I
15	HP_HAS-	I	16	HP_HCS-	I
17	HP_HCNTL1	I	18	HP_HBIL	I
19	HP_HDS2	I	20	HP_HDS1	I
21	+5 Volts	O	22	+5 Volts	O
23	HP_HRDY	O	24	HP_HPINT-	O
25	HP_HPI_EN	I	26	HP_HPI16	I
27	RESERVED		28	RESERVED	
29	RESERVED		30	RESERVED	
31	GND	O	32	GND	O
33	RESERVED		34	RESERVED	
35	RESERVED		36	RESERVED	
37	RESERVED		38	RESERVED	
39	RESERVED		40	RESERVED	
41	RESERVED		42	RESERVED	
43	RESERVED		44	RESERVED	
45	RESERVED		46	RESERVED	
47	RESERVED		48	RESERVED	
49	RESERVED		50	RESERVED	
51	GND	O	52	GND	O
53	RESERVED		54	RESERVED	
55	RESERVED		56	RESERVED	
57	RESERVED		58	RESERVED	
59	RESERVED		60	RESERVED	
61	GND	O	62	GND	O
63	HP_D7	I/O/Z	64	HP_D6	I/O/Z
65	HP_D5	I/O/Z	66	HP_D4	I/O/Z
67	HP_D3	I/O/Z	68	HP_D2	I/O/Z
69	HP_D1	I/O/Z	70	HP_D0	I/O/Z
71	GND	O	72	GND	O
73	HP_HOLDA-	O	74	HP_HOLD-	I
75	RESERVED		76	RESERVED	
77	HP_DSPIACK-	O	78	HP_RST-	O
79	GND	O	80	GND	O

2.4.5 J1, Microphone Connector

The microphone interfaces to the PCM3002E via a simple op-amp circuit. The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

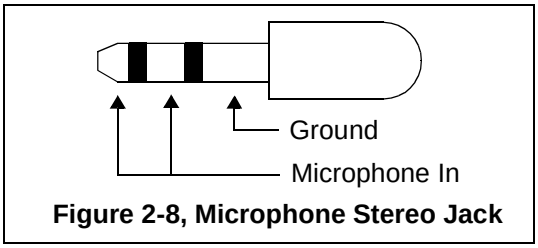


Figure 2-8, Microphone Stereo Jack

2.4.6 J2, Audio Line In Connector

The audio line in is a stereo input. This input interfaces to the PCM3002E via a simple op-amp bias circuit. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

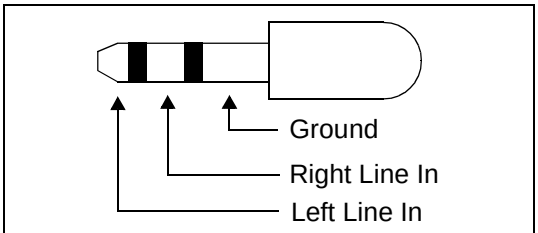


Figure 2-9, Audio Line In Stereo Jack

2.4.7 J3, Audio Line Out Connector

The audio line out is a stereo output. This output is driven by the PCM3002E through a simple op-amp circuit. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

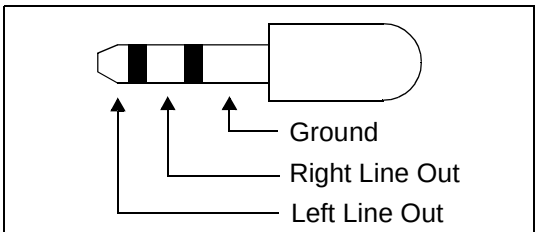


Figure 2-10, Audio Line Out Stereo Jack

2.4.8 J4, Headphone/Speaker Connector

Connector J4 is a headphone/speaker jack. It is driven by a small TPA302 amplifier connected to the PCM3002E codec and can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.

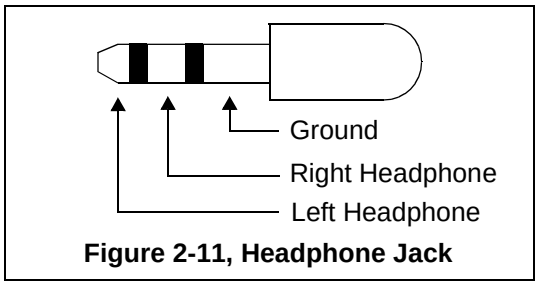


Figure 2-11, Headphone Jack

2.4.9 J5, Optional Power Connector

Connector J5 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15-24-4041. The table below shows the voltages on the respective pins.

Table 31: J5, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

2.4.10 J6, +5 Volt Connector

Power (5 volts) is brought onto the TMS320VC5416 DSK via the J6 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The The diagram of J6, which has the input power is shown below.

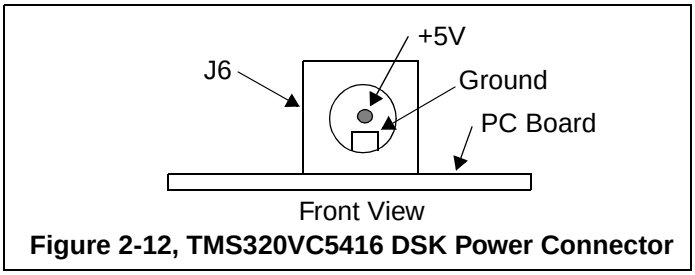


Figure 2-12, TMS320VC5416 DSK Power Connector

2.4.11 J7, External JTAG Connector

The TMS320VC5416 DSK is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-6 below.

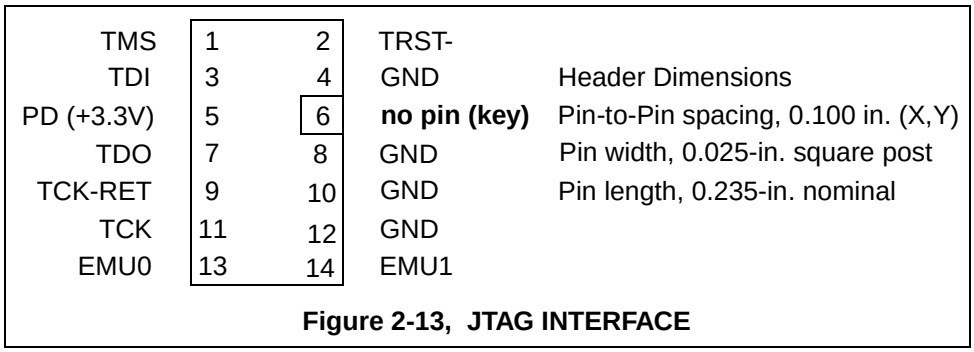


Figure 2-13, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 32: J7, JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

2.4.12 JP1, PLD Programming Connector

This connector interfaces to the Altera CPLD, U18. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

2.5 User LEDs

TheTMS320VC5416 DSK has four user definable light emitting diodes (LEDs). These LEDs are used by the Power On Self Test (POST) but are available for user programs. They are accessed via the I/O address 0x0000. The function of each LED is shown in the table below.

Table 33: User LEDs

Reference Designator	LED #	Color	Controlling Signal	On Signal State
D9	1	Green	CPLD Register 0, Data Bit 0	1
D10	2	Green	CPLD Register 0, Data Bit 1	1
D11	3	Green	CPLD Register 0, Data Bit 2	1
D12	4	Green	CPLD Register 0, Data Bit 3	1

2.5.1 System LEDs

TheTMS320VC5416 DSK has four system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

Table 34: System LEDs

Reference Designator	Color	Function	On Signal State
D6	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.	1
D7	Green	+5 Volt present	1
D8	Green	RESET Active	1
D201	Green	USB Active, Blinks during USB data transfer	1

2.6 Switches

The TMS320VC5416 has two switches, a Reset switch, and a 4 position user DIP switch.

2.6.1 Reset Switch/Reset Logic

There are three resets on the TMS320VC5416 DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5416.

External sources which control the reset are push button S1, and the on board embedded USB JTAG emulator.

2.6.2 4 Position User DIP Switch

The TMS320VC5416 DSK has a 4 position user DIP switch, S2. It is accessible via CPLD Register 0 at I/O location 0x0000. The function of each switch is shown in the table below.

Table 35: S2 Switch Positions

Position	Controlling Signal
1	CPLD Register 0, Data Bit 4
2	CPLD Register 0, Data Bit 5
3	CPLD Register 0, Data Bit 6
4	CPLD Register 0, Data Bit 7

On is a logic “1”, Off is a logic “0”.

2.7 J201, Universal Serial Bus (USB) Embedded JTAG Emulation Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

Table 36: J201, USB Connector

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

Appendix A

TMS320VC5416 DSK CPLD Equations

CPLD equations are installed in .pdf format from the CD-ROM for the DSK in the directory: C:\TI\docs\pdf\5416_dsk_vhdl.pdf

Appendix B

TMS320VC5416 DSK Schematics

This appendix contains the schematics for the TMS320VC5416 DSK. The schematics were drawn in ORCAD. Schematics for the embedded USB JTAG controller are not included.

NOTES, UNLESS OTHERWISE SPECIFIED:

1. NP = No Populate
2. RESISTANCE VALUES ARE IN OHMS.
3. CAPACITANCE VALUES ARE IN MICROFARADS.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
*	Orginal	01-09-01	
B	BETA	12-06-2001	
C	PRODUCTION	03-18-2002	

REVISION STATUS OF SHEETS

REV														
SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C

APPLICATION | NEXT ASSY | USED ON

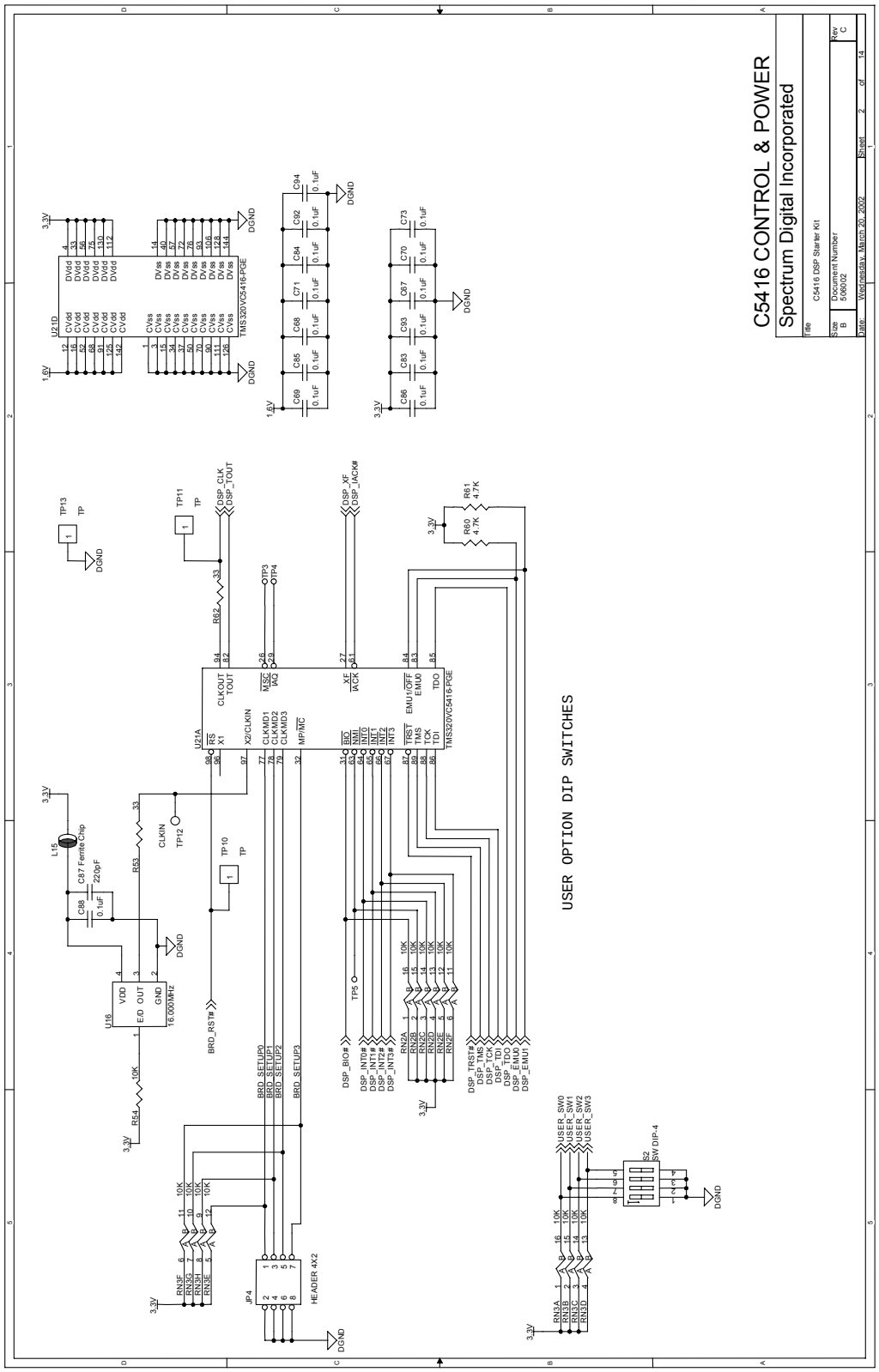
DWN DATE
CHK DATE
ENGR DATE
ENGR-MGR DATE
QA DATE
MFG DATE
RLSE DATE

Spectrum Digital Incorporated

Title: C5416 DSP Starter Kit

Size: A | Document Number: 506002 | Rev: C

Date: Wednesday, March 20, 2002 | Sheet 1 of 14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Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
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Wednesday, March 20, 2002
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TMS320VC5416-PGE
U21D
TMS320VC5416-PGE
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16.000MHz
L15
C87 Ferrite Chip
C88 0.1uF
C87 220pF
R53 33
R54 10K
R62 33
R60 4.7K
R61 4.7K
CLKIN
TP10
TP11
TP12
TP13
TP3
TP4
TP5
JP4
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DSP_TDO
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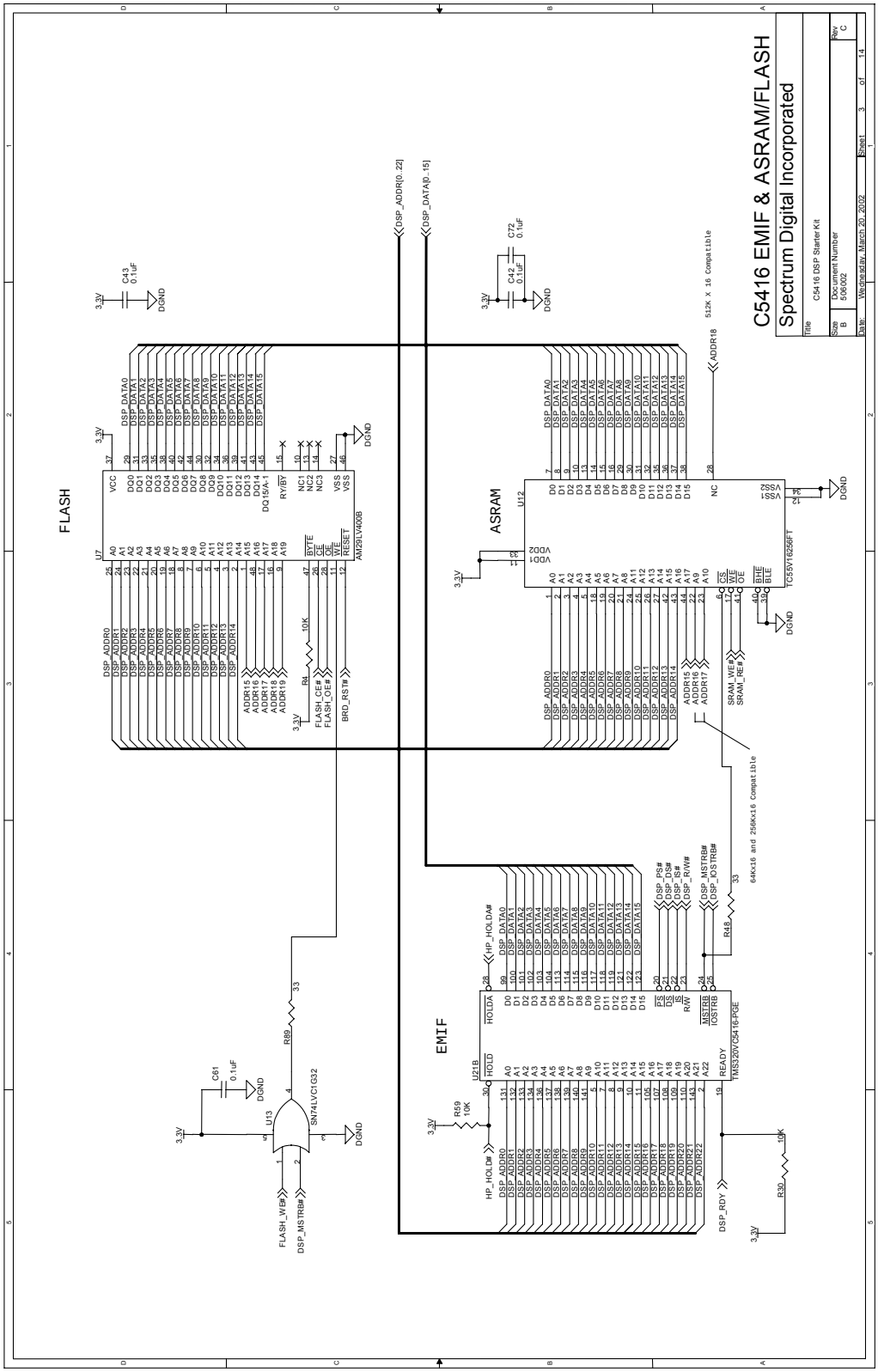
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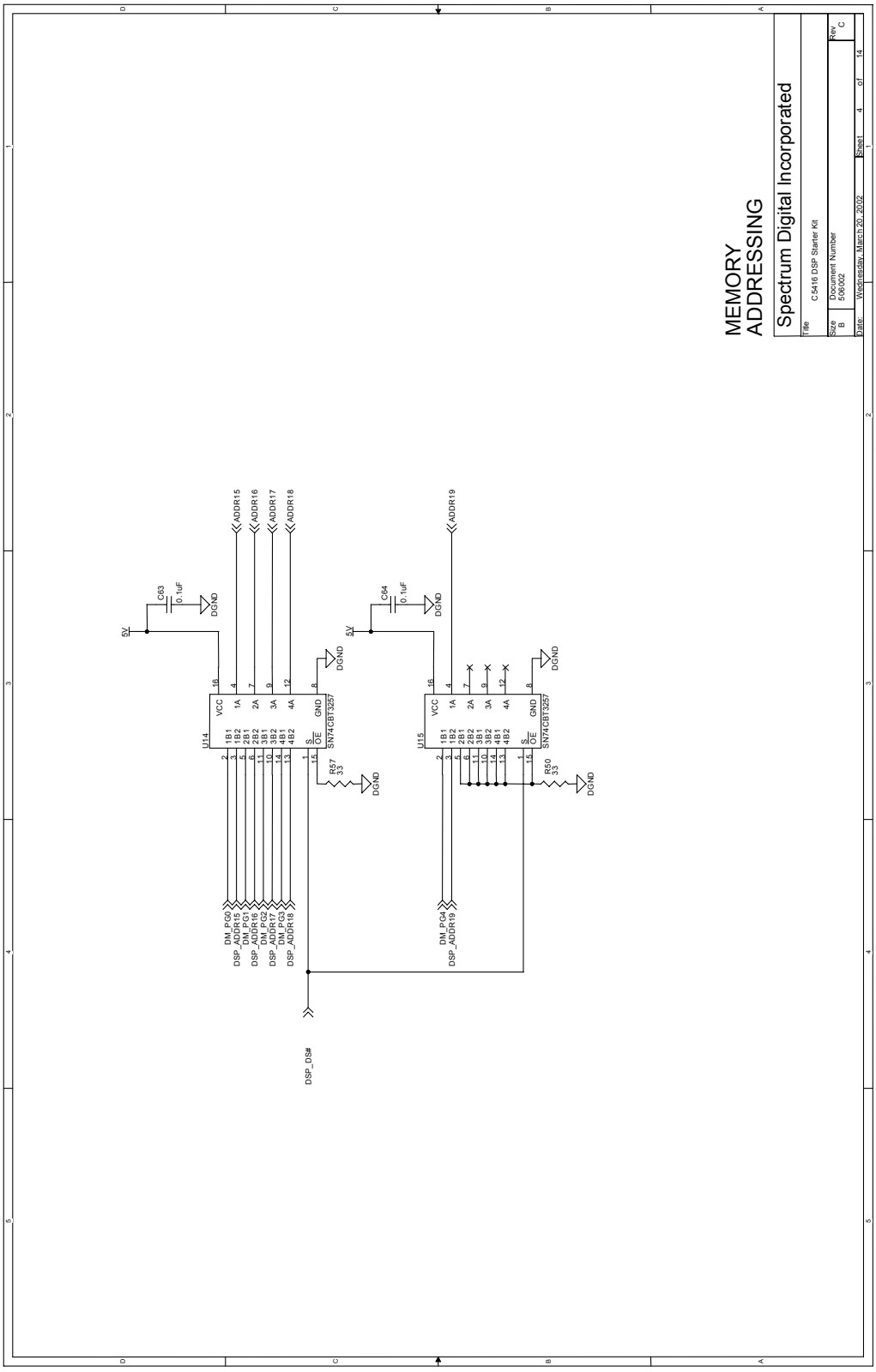
TC55V16256FT
SN74LVC1G32
512K X 16 Compatible
64Kx16 and 256Kx16 Compatible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Rev
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2OE
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2A
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4A
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2B2
3B1
3B2
4B1
4B2
C63
0.1uF
C64
0.1uF
5V
DGND
ADDR15
ADDR16
ADDR17
ADDR18
ADDR19
R57
33
R60
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DM_PG0
DSP_ADDR15
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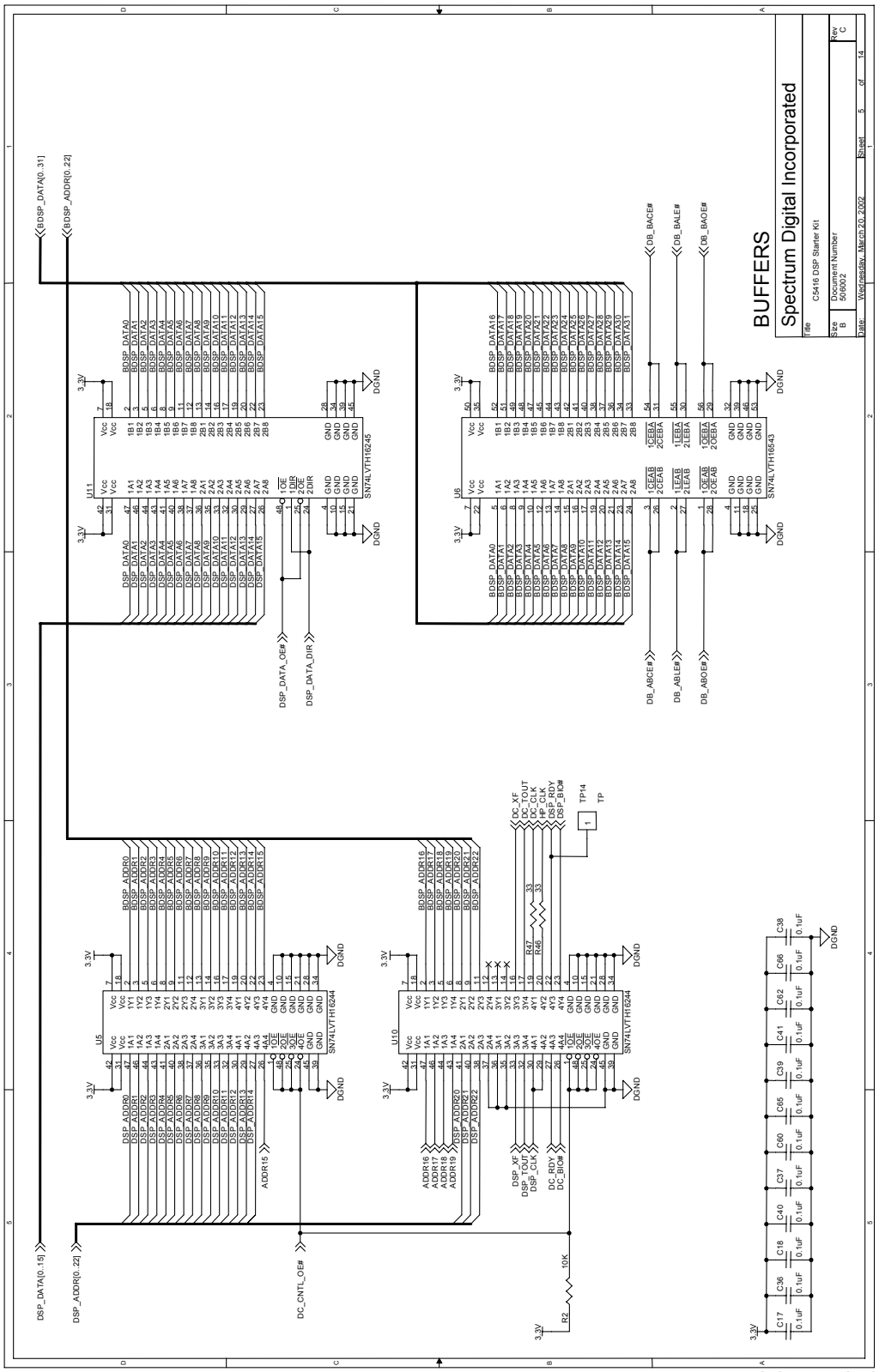
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DGND
R2 10K
R47 33
R46 33
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C36 0.1uF
C18 0.1uF
C40 0.1uF
C37 0.1uF
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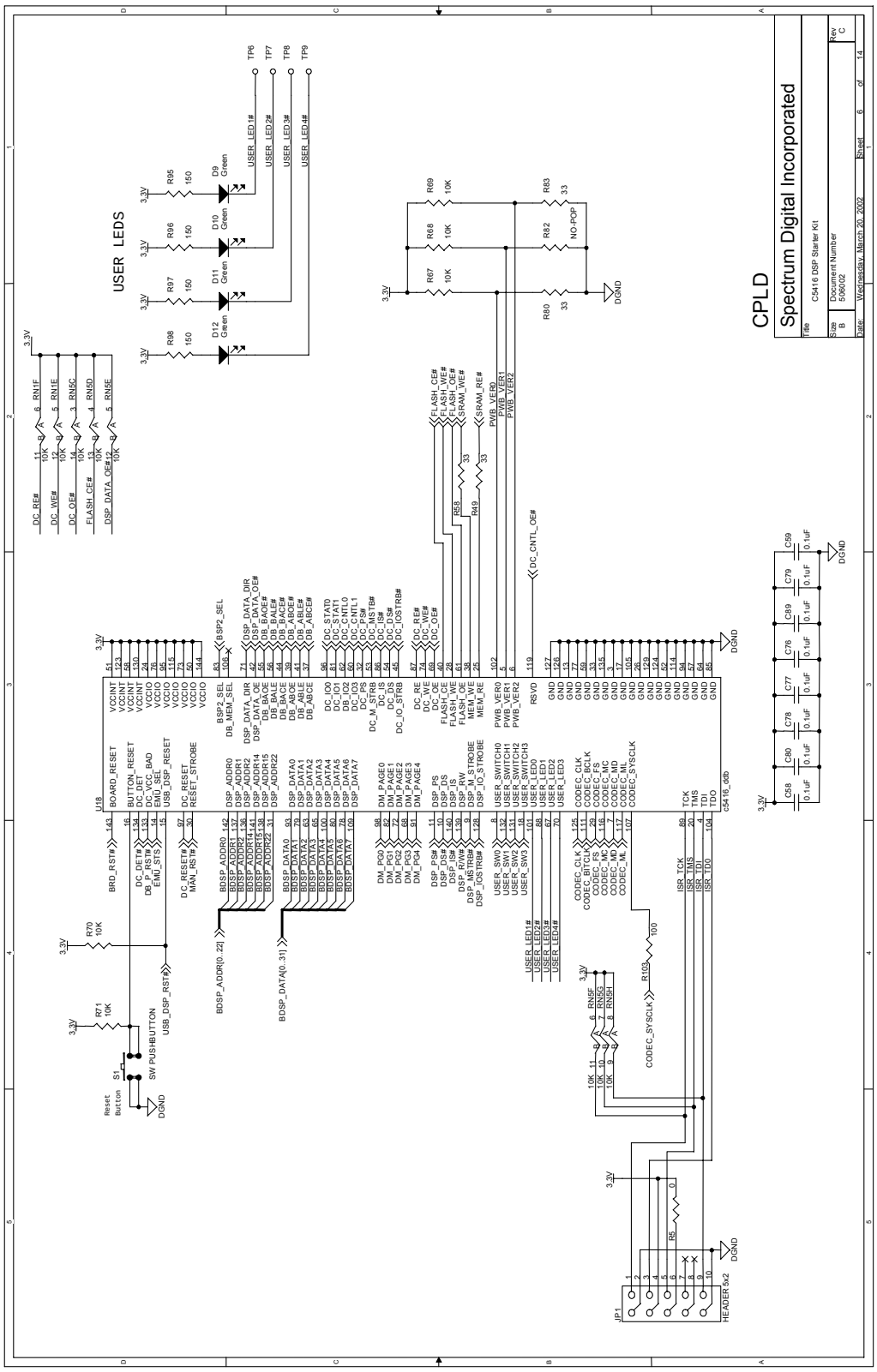
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USER_LED3#
USER_LED4#
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DC_WE#
DC_OE#
FLASH_CE#
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U18
BOARD_RESET
BUTTON_RESET
DC_DET
DC_CNTL_BAD
EMU_SEL
USB_DSP_RESET
DC_RESET
RESET_STROBE
DC_RESET#
MAN_RST#
BSP2_SEL
DB_MEM_SEL
DSP_DATA_DIR
DSP_DATA_OE#
DB_BACE
DB_BALE#
DB_BACE#
DB_ABLE#
DB_ABCE#
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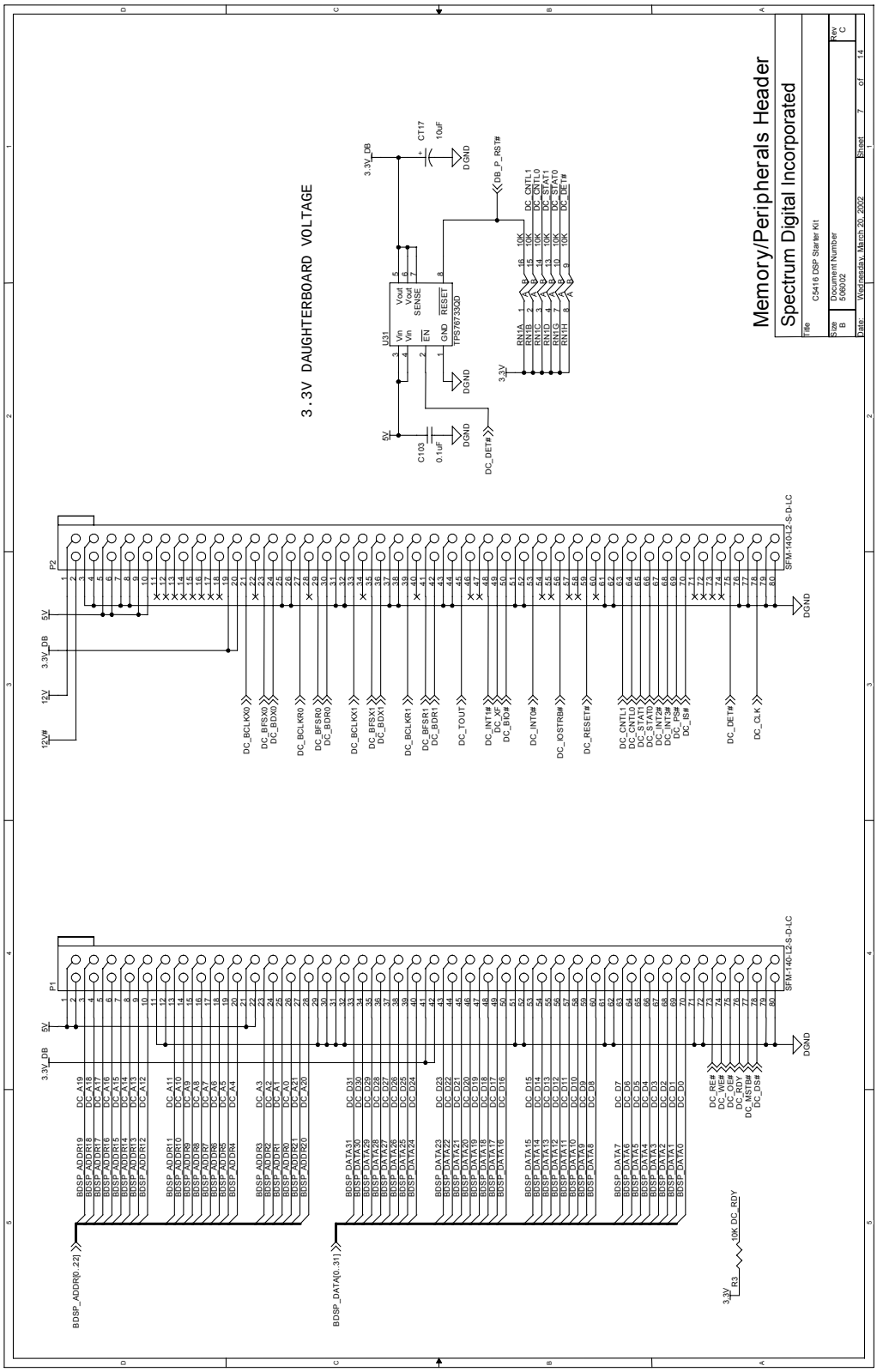
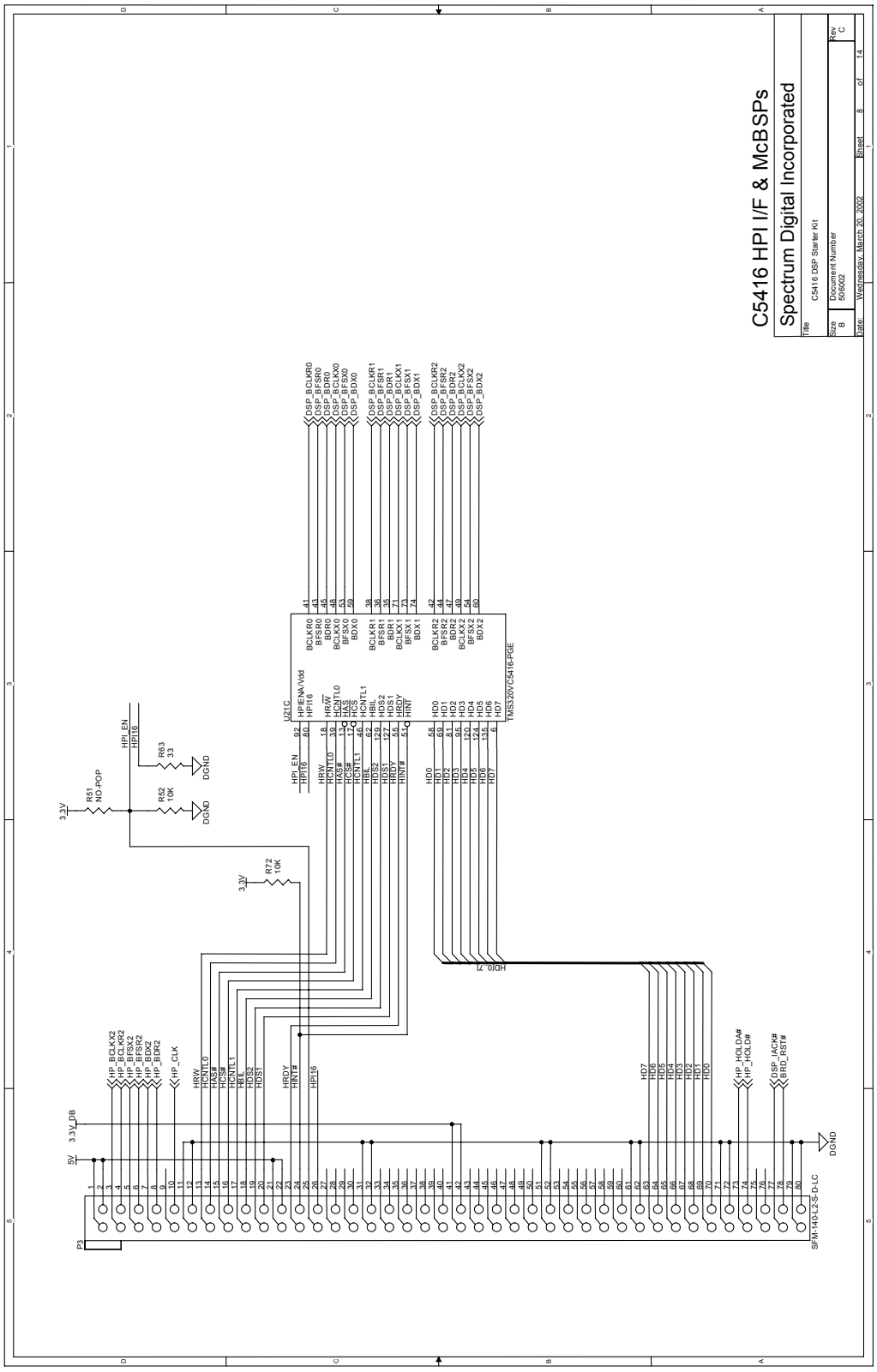
DC_STAT1
DC_CNTL0
DC_CNTL1
DC_CNTL2
DC_MSTB#
DC_IS#
DC_DS#
DC_IOSTRB#
DC_RE#
DC_WE#
DC_OE#
FLASH_CE#
FLASH_WE#
FLASH_OE#
SRAM_WE#
MEM_RE#
SRAM_RE#
PWB_VER0
PWB_VER1
PWB_VER2
RSVD
BDSP_ADDR[0..22]
BDSP_DATA[0..31]
DSP_ADDR0
DSP_ADDR1
DSP_ADDR2
DSP_ADDR14
DSP_ADDR15
DSP_ADDR22
DSP_DATA0
DSP_DATA1
DSP_DATA2
DSP_DATA3
DSP_DATA4
DSP_DATA5
DSP_DATA6
DSP_DATA7
DM_PG0
DM_PG1
DM_PG2
DM_PG3
DM_PG4
DM_PAGE0
DM_PAGE1
DM_PAGE2
DM_PAGE3
DM_PAGE4
DSP_PS
DSP_DS
DSP_IS
DSP_RW
DSP_MSTROBE
DSP_IOSTRB
USER_SW0
USER_SW1
USER_SW2
USER_SW3
USER_SWITCH0
USER_SWITCH1
USER_SWITCH2
USER_SWITCH3
USER_LED0
USER_LED1
USER_LED2
USER_LED3
GND
CODEC_CLK
CODEC_BCLK
CODEC_FS
CODEC_MC
CODEC_MD
CODEC_ML
CODEC_SYSCLK
TCK
TMS
TDI
TDO
c54 16_ddb
ISR_TCK
ISR_TMS
ISR_TDI
ISR_TDO
D9 Green
D10 Green
D11 Green
D12 Green
R95 150
R96 150
R97 150
R98 150
R68 10K
R69 10K
R67 10K
R83 33
R82 NO-POP
R80 33
R58 33
R49 33
R70 10K
R71 10K
R5 0
R103 100
RN1F 10K
RN1E 10K
RN5C 10K
RN5D 10K
RN5E 10K
RN5F 10K
RN5G 10K
RN5H 10K
TP6
TP7
TP8
TP9
C68 0.1uF
C80 0.1uF
C78 0.1uF
C77 0.1uF
C76 0.1uF
C89 0.1uF
C79 0.1uF
C69 0.1uF
S1
Reset Button
3.3V
DGND


Memory/Peripherals Header
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
506002
Wednesday, March 20, 2002
3.3V DAUGHTERBOARD VOLTAGE
P1
P2
SFM-140-L2-S-D-LC
U31
TPS767330D
DGND
3.3V_DB
5V
12V
12V#
DC_DET#
DB_P_RST#
BDSP_ADDR[0..22]
BDSP_DATA[0..31]
10K DC_RDY
DC_CLK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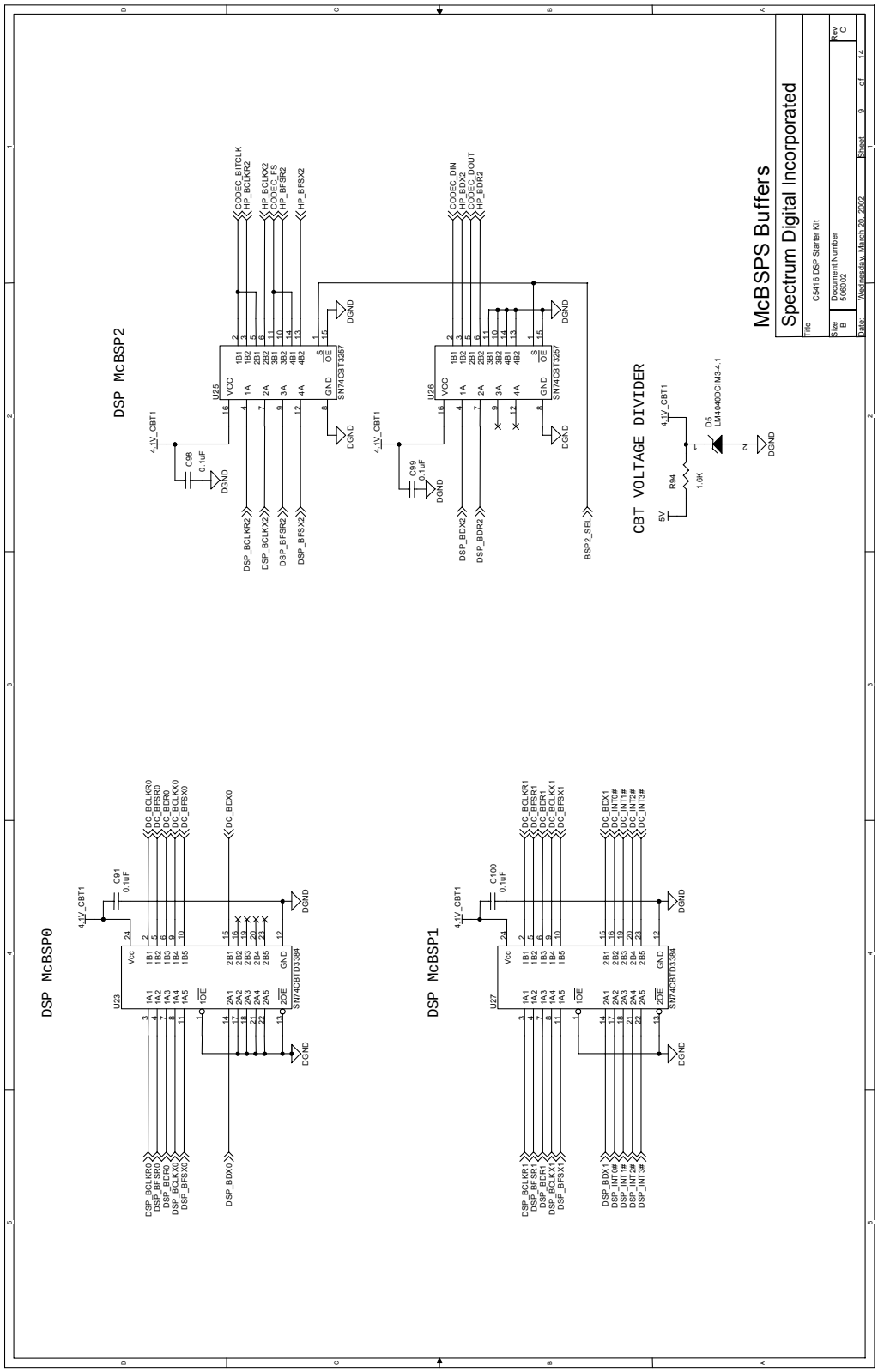
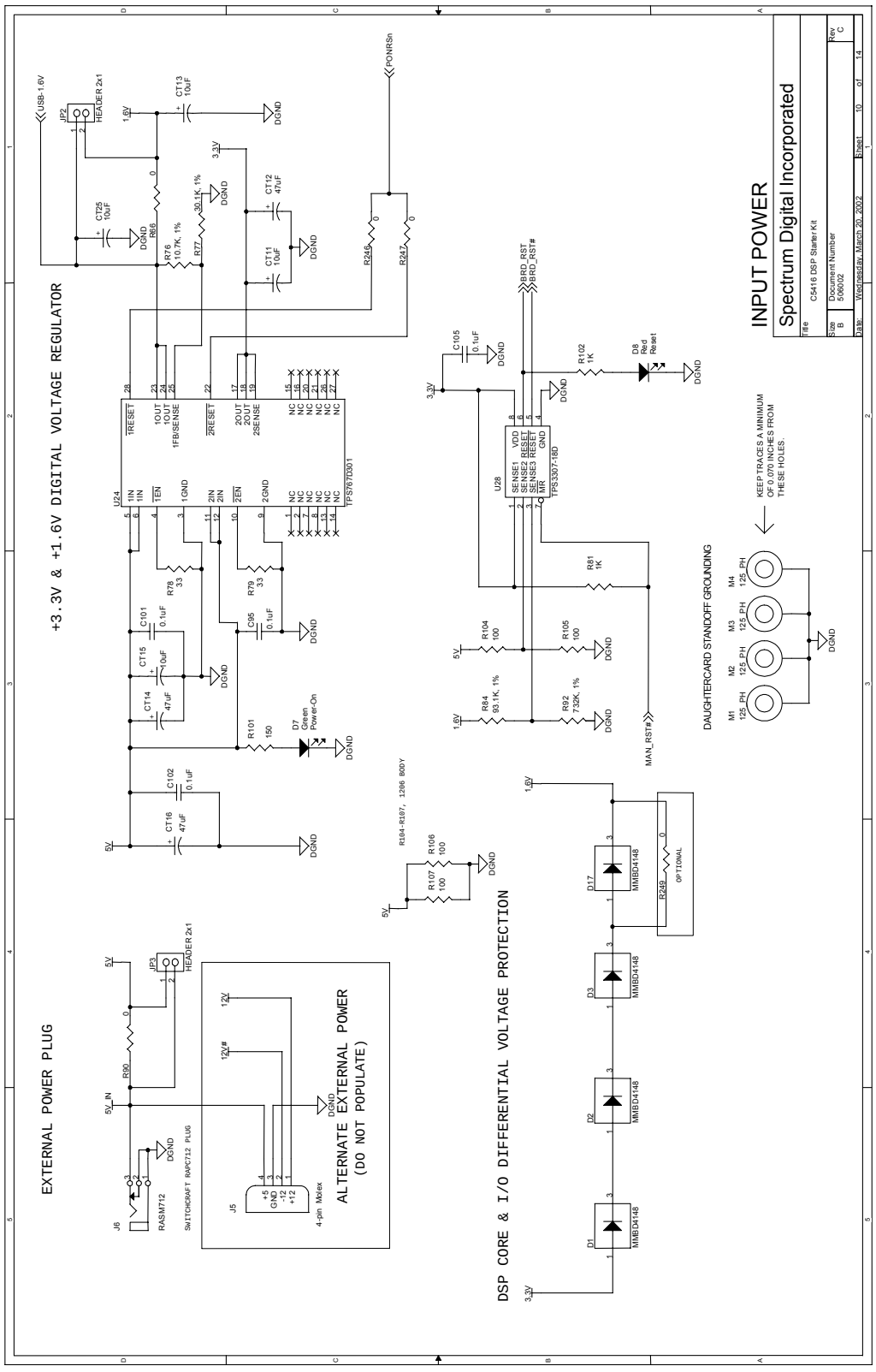
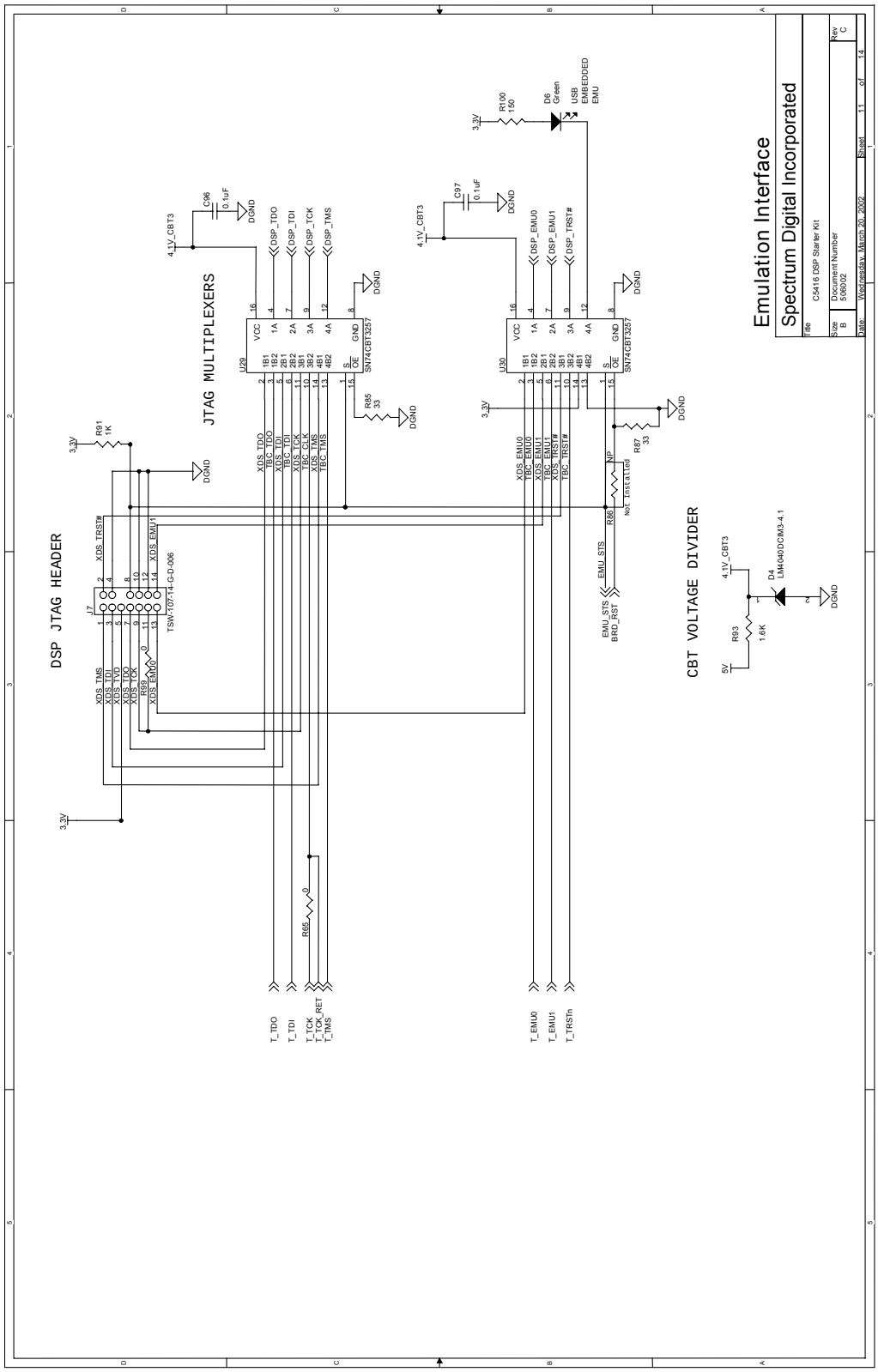
Spectrum Digital Incorporated
Title
C5416 DSP Starter Kit
Size
B
Document Number
506002
Rev
C
Date:
Wednesday, March 20, 2002
Sheet
8
of
14
U21C
TMS320VC5416-PGE
P3
SFM-140-L2-S-D-LC
R61
NO-POP
R62
10K
R63
33
R72
10K
3.3V
5V
DGND
HPI_EN
HPI16
HRW
HCNTL0
HAS#
HCS#
HCNTL1
HBIL
HDS2
HDS1
HRDY
HINT#
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
HD[0..7]
HP_BCLKX2
HP_BCLKR2
HP_BFSX2
HP_BFSR2
HP_BDX2
HP_BDR2
HP_CLK
HP_HOLD#
HP_HOLDA#
DSP_IACK#
DSP_RST#
3.3V_DB


McBSPS Buffers
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
5060l02
Wednesday, March 20, 2002
DSP McBSP2
DSP McBSP0
DSP McBSP1
CBT VOLTAGE DIVIDER
SN74CBT3257
SN74CBTD3384
4.1V_CBT1
DGND
BSP2_SEL


+3.3V & +1.6V DIGITAL VOLTAGE REGULATOR
EXTERNAL POWER PLUG
ALTERNATE EXTERNAL POWER
(DO NOT POPULATE)
DSP CORE & I/O DIFFERENTIAL VOLTAGE PROTECTION
DAUGHTERCARD STANDOFF GROUNDING
KEEP TRACES A MINIMUM OF 0.070 INCHES FROM THESE HOLES.
INPUT POWER
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
Wednesday, March 20, 2002
TPS767D301
TPS3307-18D
SWITCHCRAFT RAPC712 PLUG
4-pin Molex
MMBD4148
HEADER 2x1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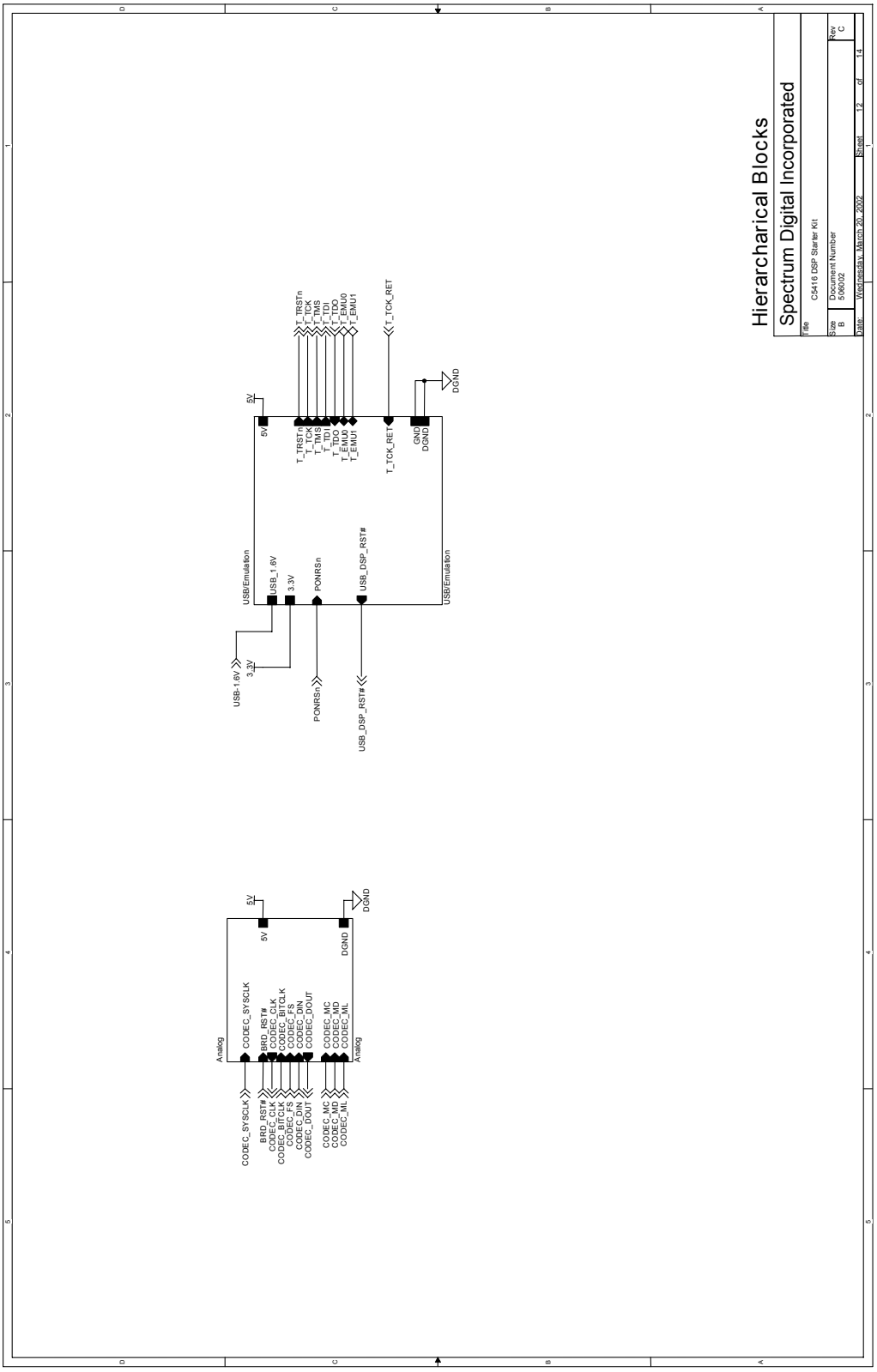
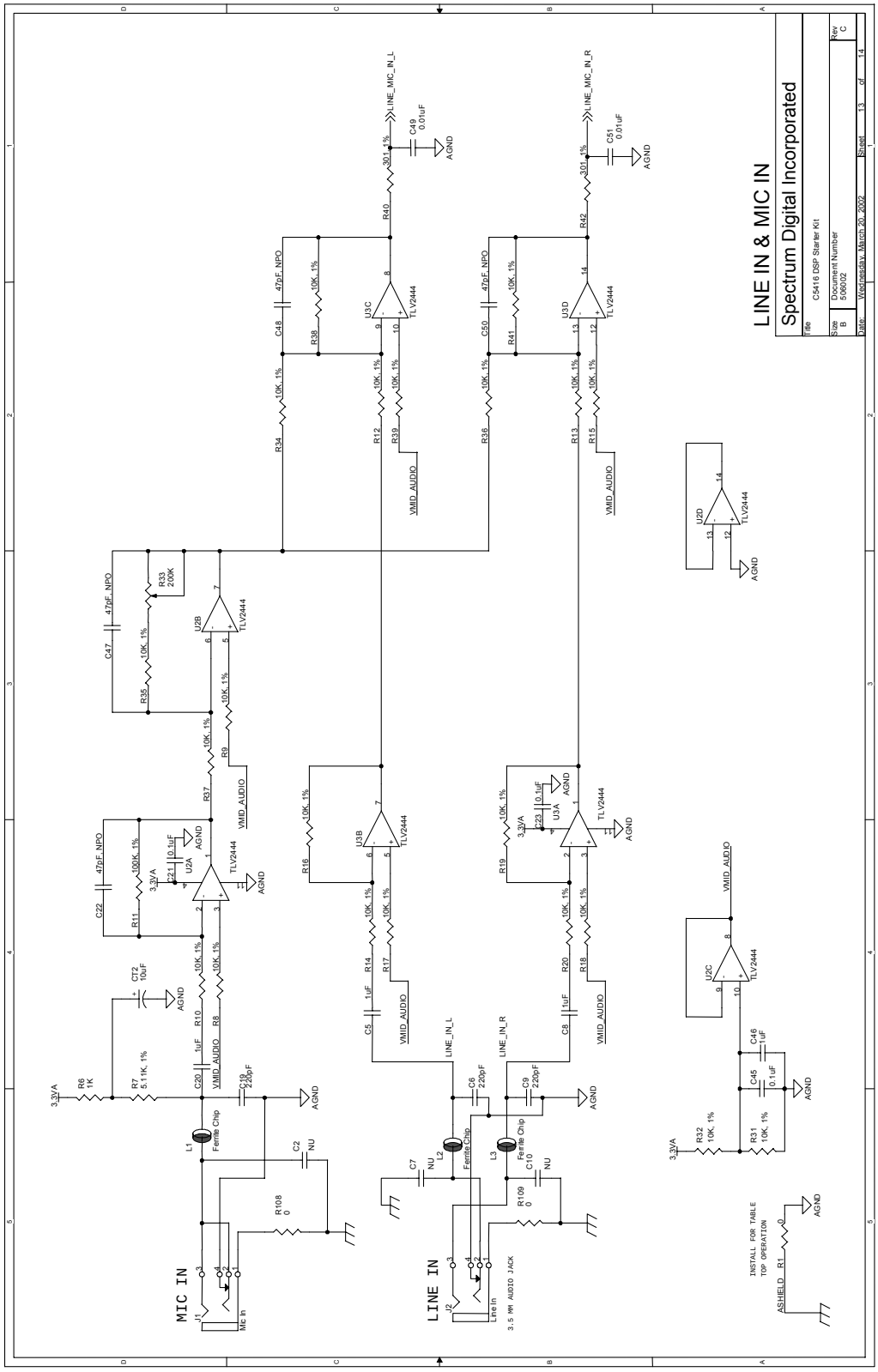
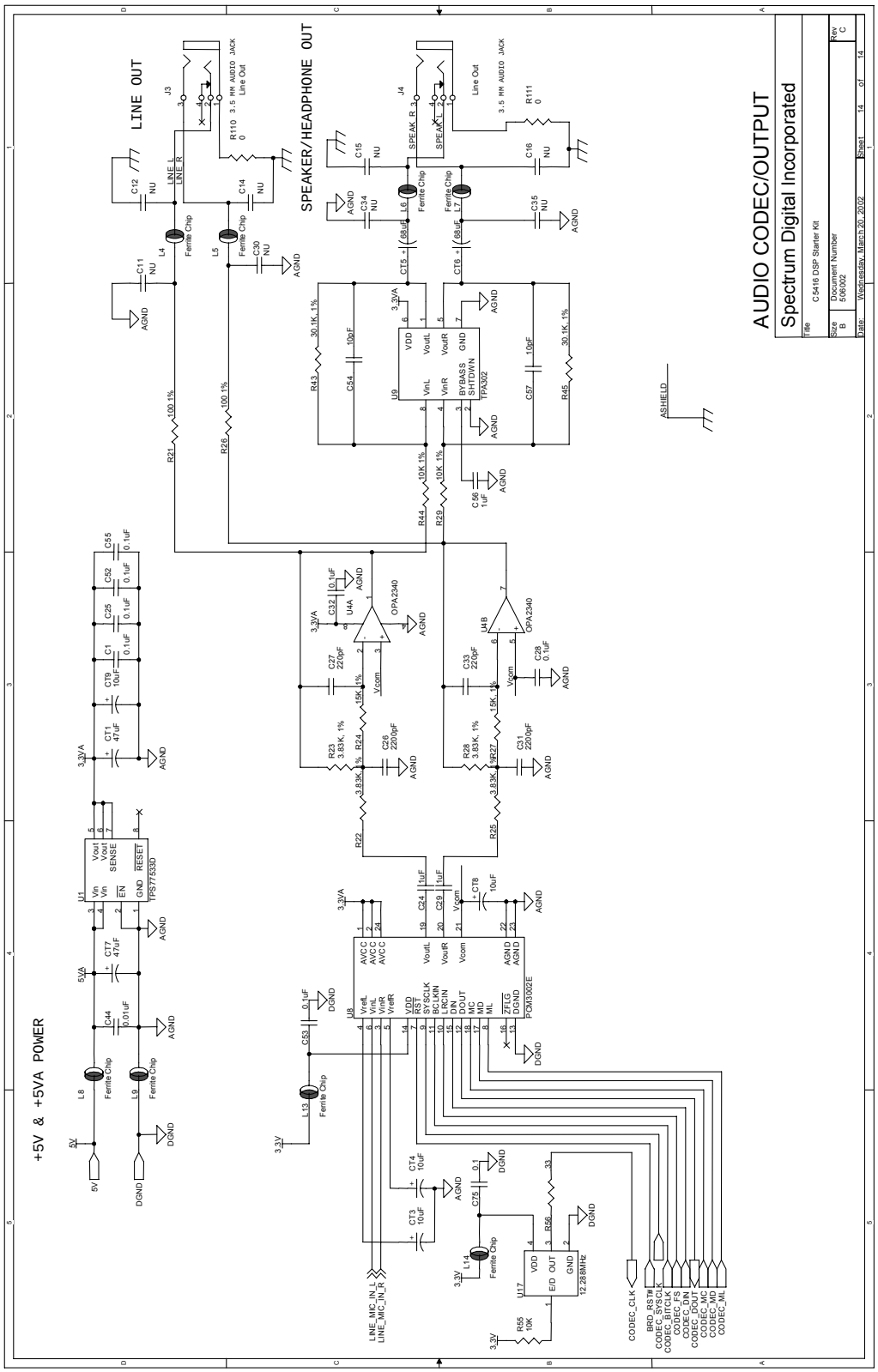
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
5060J2
Wednesday, March 20, 2002
JTAG MULTIPLEXERS
DSP JTAG HEADER
CBT VOLTAGE DIVIDER
TSW-107-14-G-D-006
SN74CBT3257
LM4040DCIM3-4.1
USB EMBEDDED EMU
Not Installed
XDS_TMS
XDS_TDI
XDS_TVD
XDS_TDO
XDS_TCK
XDS_RTCK
XDS_EMU0
XDS_TRST#
XDS_EMU1
DSP_TDO
DSP_TDI
DSP_TCK
DSP_TMS
DSP_EMU0
DSP_EMU1
DSP_TRST#
TBC_TDO
TBC_TDI
TBC_CLK
TBC_TMS
TBC_EMU0
TBC_EMU1
TBC_TRST#
EMU_STS
BRD_RST
T_TDO
T_TDI
T_TCK
T_TCK_RET
T_TMS
T_EMU0
T_EMU1
T_TRSTn
4.1V_CBT3
3.3V
5V
DGND


Hierarcharical Blocks
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
506002
Rev C
Wednesday, March 20, 2002
Sheet 12 of 14
USB/Emulation
5V
DGND
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TCK_RET
USB_1.6V
3.3V
PONRSn
USB_DSP_RST#
Analog
CODEC_SYSCLK
BRD_RST#
CODEC_CLK
CODEC_BITCLK
CODEC_FS
CODEC_DIN
CODEC_DOUT
CODEC_MC
CODEC_MD
CODEC_ML


LINE IN & MIC IN
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
5060/02
Wednesday, March 20, 2002
MIC IN
LINE IN
INSTALL FOR TABLE TOP OPERATION
LINE_MIC_IN_L
LINE_MIC_IN_R
VMID_AUDIO
LINE_IN_L
LINE_IN_R
AGND
3.3VA
TLV2444
Ferrite Chip


AUDIO CODEC/OUTPUT
Spectrum Digital Incorporated
C5416 DSP Starter Kit
Document Number
506102
Wednesday, March 20, 2002
LINE OUT
SPEAKER/HEADPHONE OUT
+5V & +5VA POWER
TPS77533D
PCM3002E
OPA2340
TPA032
12.288Mhz
Ferrite Chip
3.5 MM AUDIO JACK
LINE_MIC_IN_L
LINE_MIC_IN_R
CODEC_CLK
BRD_RST#
CODEC_SYSCLK
CODEC_BITCLK
CODEC_FS
CODEC_DIN
CODEC_DOUT
CODEC_MC
CODEC_MD
CODEC_ML

Appendix C

TMS320VC5416 DSK List of materials

This appendix contains the list of materials for the TMS320VC5416 DSK.

Table 1: TMS320VC5416 List of Materials

Item	Qty	Title	Mfr Name	PWB Ref #	Mfr P/N
1	1	PWB,TMS320VC5416 USB DSK	SPECTRUM DIGITAL, INC.		
2	1	LOGIC,TMS320VC5416 USB DSK	SPECTRUM DIGITAL, INC.		
3	1	ASSY,EMBEDDED USB EMULATOR	SPECTRUM DIGITAL, INC.		
4	1	FPGA	ALTERA	U18	EPM3128ATC144-10
5	1	IC,PQFP,TMS320VC5416 PGE-160	TEXAS INSTRUMENTS	U21	TMS320VC5416PGE-160
6	1	IC,TSOP44,SRAM,64K x 16,12nS	ISSI	U12	IS61LV6416-12T
7	1	IC,TSOP48,FLASH,70nS	ADVANCED MICRO DEVICES, INC	U7	AM29LV400BT-70EC
8	1	IC,TSSOP48,3.3V,16-BIT TRANSCEIVER	TEXAS INSTRUMENTS	U11	SN74LVTH16245ADGGR
9	2	IC,TSSOP48,3.3V,16-BIT BUFFER/DRIVER	TEXAS INSTRUMENTS	U5,U10	SN74LVTH16244ADGGR
10	1	IC,TSSOP56,3.3V,16-BIT TRANSCEIVER	TEXAS INSTRUMENTS	U6	SN74LVTH16543DGGR
11	2	IC,TSSOP24,10-BIT FET BUS SWITCH,74CBTS3384	TEXAS INSTRUMENTS	U23,U27	SN74CBTS3384PW
12	1	IC,MSOP8,OP AMP	BURR-BROWN CORPORATION	U4	OPA2340EA/250
13	6	IC,QSOP16,QUAD 2:1 MULTIPLEXER / DEMULTIPLEXER	QUALITY SEMICONDUCTOR INC.	U14,U15,U25,U26, U29,U30	QS3257Q
14	1	IC,SSOP24,STEREO AUDIO CODEC	BURR-BROWN CORPORATION	U8	PCM3002E
15	1	IC,SO8,STEREO AUDIO POWER AMPLIFIER,300mW	TEXAS INSTRUMENTS	U9	TPA302D
16	2	IC,TSSOP14,OP AMP, LOW VOLTAGE	TEXAS INSTRUMENTS	U2,U3	TLV2444CPWR
17	1	IC,SOIC,3.3V,1A LOW-DROPOUT VOLTAGE REGULATOR,TPS76733	TEXAS INSTRUMENTS	U31	TPS76733QD
18	1	IC,SOIC,3.3V,500mA LOW-DROPOUT VOLTAGE REGULATOR,TPS77533	TEXAS INSTRUMENTS	U1	TPS77533D
19	1	IC,SSOP28,DUAL LOW-DROPOUT VOLTAGE REGULATOR	TEXAS INSTRUMENTS	U24	TPS767D301PWP
20	1	IC,SO8,TRIPLE SUPERVI-SORY CIRCUIT,3.3V	TEXAS INSTRUMENTS	U28	TPS3307-18D
21	1	IC,SOT23-5,SINGLE CMOS OR GATE	TEXAS INSTRUMENTS	U13	SN74LVC1632DBBK
22	1	OSC,SMT,12.288 MHZ	CTS ELECTRONICS CORPORATION	U17	CB3LV-3C-12.288T
23	1	OSC,SMT,16 MHZ	CTS ELECTRONICS CORPORATION	U16	CB3LV-3C-16.000T

Table 1: TMS320VC5416 List of Materials

Item	Qty	Title	Mfr Name	PWB Ref #	Mfr P/N
24	2	DIODE,SOT23, REFERENCE,4.1V	NATIONAL SEMICON-DUCTOR	D4,D5	LM4040CIM3-4.1
25	4	DIODE,SOT23, SWITCHING	ZETEX INC.	D1,D2,D3,D17	BAS16TA
26	1	LED,SMT 1206,YELLOW	LUMEX, INC.	D8	SML-LX1206YC-TR
27	6	LED,SMT 1206,GREEN	LITEON	D6,D7,D9,D10, D11,D12	LTST-C150GKT
28	12	FERRITE BEAD,SMT 0805,600 OHMS	STEWARD	L1,L2,L3,L4,L5,L6, L7,L8,L9,L13,L14, L15	HZ0805E601R-00
29	2	CAP,CER,SMT 0603,10pF,50V, +/-.5pF,NPO	PANASONIC	C54,C57	ECU-V1H100DCV
30	4	CAP,CER,SMT 0603,47pF,50V, +/-5%,NPO	PANASONIC	C22,C47,C48,C50	ECU-V1H470JCV
31	2	CAP,CER,SMT 0603,2200pF,50V, +/-10%,X7R	PANASONIC	C26,C31	ECUV1H222KBV
32	6	CAP,CER,SMT 0603,220pF,50V, +/-5%,NPO	PANASONIC	C6,C9,C19,C27, C33,C87	ECU-V1H221JCV
33	4	CAP,CER,SMT 0603,.01uF,50V, +/-10%,X7R	AVX CORPORATION	C44,C49,C51,C104	06035C103KAT2A
34	63	CAP,CER,SMT 0603,.1uF,16V, +/-10%,X7R	PANASONIC	C1,C17,C18,C21, C23,C25,C28,C32, C36,C37,C38,C39, C40,C41,C42,C43, C45,C52,C53,C55, C58,C59,C60,C61, C62,C63,C64,C65, C66,C67,C68,C69, C70,C71,C72,C73, C74,C75,C76,C77, C78,C79,C80,C83, C84,C85,C86,C88, C89,C91,C92,C93, C94,C95,C96,C97, C98,C99,C100, C101,C102,C103, C105	ECJ-1VB1C104K
35	7	CAP,CER,SMT 0603,1uF,6.3V,X5R, +/-10%	PANASONIC	C5,C8,C20,C24, C29,C46,C56	ECJ-1VB0J105K
36	12	CAP,TANT,TEH SERIES,SMT 1206,10uF,6.3V	PANASONIC	CT2,CT3,CT4,CT8, CT9,CT11,CT13, CT15,CT17,CT23, CT24,CT25	ECS-TOJY106R
37	2	CAP,TANT,SMT 2816,68uF,6.3V	PANASONIC	CT5,CT6	ECS-T0JY106R
38	5	CAP,TANT,SMT 2816,47uF,10V	PANASONIC	CT1,CT7,CT12, CT14,CT16	ECS-T1AD476R
39	4	RES,SMT,1206 120 OHM, 5%, 1/4 WATT	PANASONIC	R104,R105,R106, R107	ERJ-8GEYJ121V
40	3	RES,SMT 0603,100 OHM,1%,1/16 WATT	ROHM CORPORATION	R21,R26,R103	MCR03F1000EZP

Table 1: TMS320VC5416 List of Materials

Item	Qty	Title	Mfr Name	PWB Ref #	Mfr P/N
41	22	RES,SMT 0603,10K OHM,1%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R8,R9,R10,R12, R13,R14,R15,R16, R17,R18,R19,R20, R29,R31,R32,R34, R35,R36,R37,R38, R39,R41,R44	RK73H1J1002F
42	1	RES,SMT 0603,100K OHM,1%,1/10 WATT	ROHM CORPORATION	R11	MCR03F1003EZP
43	1	RES,SMT 0603,10.7K OHM,1%,1/16 WATT	PANASONIC	R76	ERJ-3EKF1072V
44	2	RES,SMT 0603,200K OHM,1%,1/10 WATT	PANASONIC	R43,R45	ERJ-3EKF2003V
45	2	RES,SMT 0603,301 OHM,1%,1/16 WATT	PANASONIC	R40,R42	ERJ-3EKF3010V
46	4	RES,SMT 0603,3.83K OHM,1%,1/10 WAT”	PANASONIC	R22,R23,R25,R28	ERJ-3EKF3831V
47	1	RES,SMT 0603,30.1K OHM,1%,1/10 WATT	PANASONIC	R77	ERJ-3EKF3012V
48	1	RES,SMT 0603,5.11K OHM,1%,1/10 WATT	PANASONIC	R7	ERJ-3EKF5111V
49	2	RES,SMT 0603,15K OHM,1%,1/16 WAT”	PANASONIC	R24,R27	ERJ-3EKF1502V
50	1	RES,SMT 0603,732K OHM,1%,1/10 WATT	PANASONIC	R92	ERJ-3EKF7323V
51	1	RES,SMT 0603,93.1K OHM,1%,1/10 WATT	PANASONIC	R84	ERJ-3EKF9312V
52	8	RES,SMT 0603,0 OHM, 1/10 WATT	KOA SPEER ELECTRONICS, INC.	R5,R65,R86,R99, R108,R109,R110, R111	RM73Z1J000
53	4	RES,SMT 0603,1K OHM,5%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R6,R81,R91,R102	RM73B1JT102J
54	14	RES,SMT 0603,10K OHM,5%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R2,R3,R4,R30, R51,R54,R55,R59, R67,R68,R69,R70, R71,R72	RM73B1JT103J
55	2	RES,SMT 0603,1.6K OHM,5%,1/16 WATT	PANASONIC	R93,R94	ERJ-3GEYJ162V
56	6	RES,SMT 0603,150 OHM,5%,1/16 WATT	PANASONIC	R95,R96,R97,R98, R100,R101	ERJ-3GEYJ151V
57	19	RES,SMT 0603,33 OHM,5%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R46,R47,R48,R49, R50,R52,R53,R56, R57,R58,R62,R63, R78,R79,R82,R83, R85,R87,R89	RM73B1JT33RJ
58	2	RES,SMT 0603,4.7K OHM,5%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R60,R61	RM73B1JT472J
59	2	RES,SMT 0603,20K OHM,5%,1/16 WATT	KOA SPEER ELECTRONICS, INC.	R29,R44	RM73B1JT203J
60	3	RES,SMT 1206,0 OHM, 1/8 WATT	XICON PASSIVE COMPONENTS	R1,R66,R90	263-0
61	1	POT,SMT,5mm SQ.,200K,1/4 WATT, SINGLE TURN	BOURNS	R33	3314J-1-204
62	5	RES,NETWORK,SMT, 16 PIN,8 RES,10K OHM,5%,1/16 WATT	CTS ELECTRONICS CORPORATION	RN1,RN2,RN3, RN4,RN5	742163103J

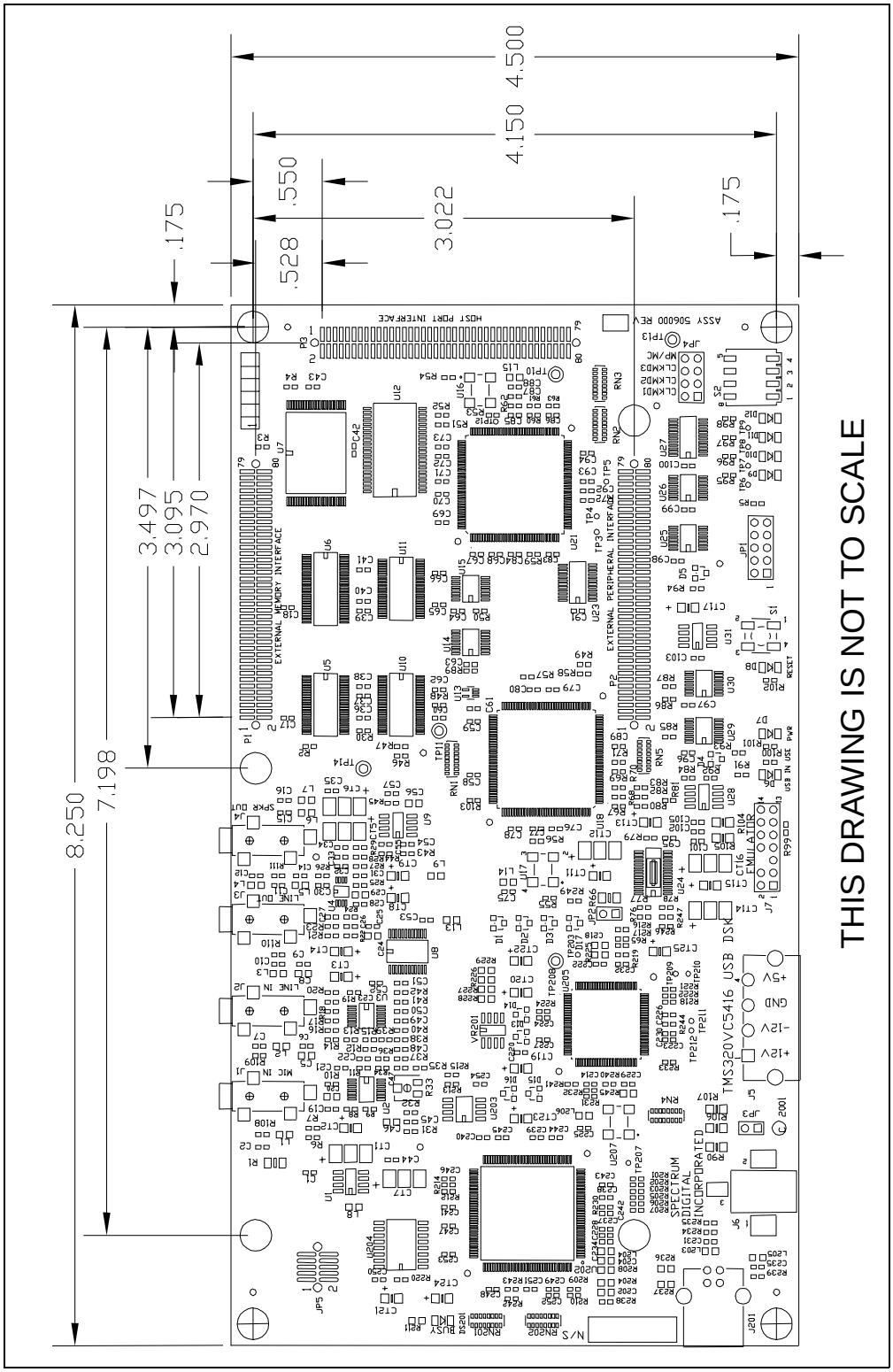
Table 1: TMS320VC5416 List of Materials

Item	Qty	Title	Mfr Name	PWB Ref #	Mfr P/N
63	1	SWITCH,SMT, PUSHBUTTON, MOMENTARY,.25 SQ.	C&K/UNIMAX, INC.	S1	KT11P2JM
64	1	SWITCH,DIP,SMT, 4 POSITION	CTS ELECTRONICS CORPORATION	S2	193-MS
65	1	HEADER,4 X 2, VERTICAL,PIN	SPECTRUM DIGITAL INC.	JP4	
66	1	HEADER,5 X 2, VERTICAL,PIN	SPECTRUM DIGITAL INC.	JP1	
67	1	HEADER,7 X 2, VERTICAL,PIN	SPECTRUM DIGITAL INC.	J7	
68	1	CONN,JACK,RIGHT ANGLE,POWER,2.5mm	SWITCHCRAFT	J6	RASM712
69	3	CONN,SMT, VERTICAL, RECEPTACLE,40X2	AMP INCORPORATED	P1,P2,P3	104652-8
70	4	CONN,SMT,JACK, STEREO,4 POS.,3.6mm	KYCON CABLE & CONNECTOR, INC.	J1,J2,J3,J4	ST-3500-4N
71	4	BUMPER, CYLINDRICAL,SELF-STICK,BLACK,.88 DIA.	3M ELECTRONIC PRODUCTS DIV.		SJ-5009(BLACK)

Appendix D

TMS320VC5416 DSK Mechanical Information

This appendix contains the mechanical information about the TMS320VC5416 DSK produced by Spectrum Digital.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Printed in U.S.A., March 2002
506005-0001 Rev. A