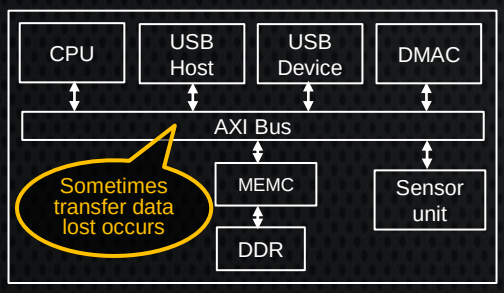
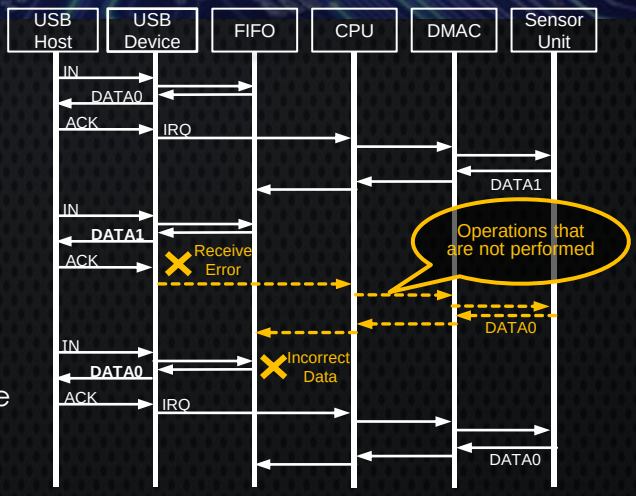
VSTAR™ FPGA Design Auto-Debugger

The industry's only solution for FPGA design auto-debug with reconfigurable on-chip verification IP and proprietary GUI. VSTAR auto-generates rules in real time for the signal state transitions with the patent-pending technology to eliminate the need for user defined trigger conditions and free users from multiple iterations of FPGA P&R and execution. It's easy to debug with narrowing down from auto-detected errors at system level to the detailed debug on waveform. System level operation can be displayed up to 100,000x longer than waveform to clearly show before and after error occurrence.

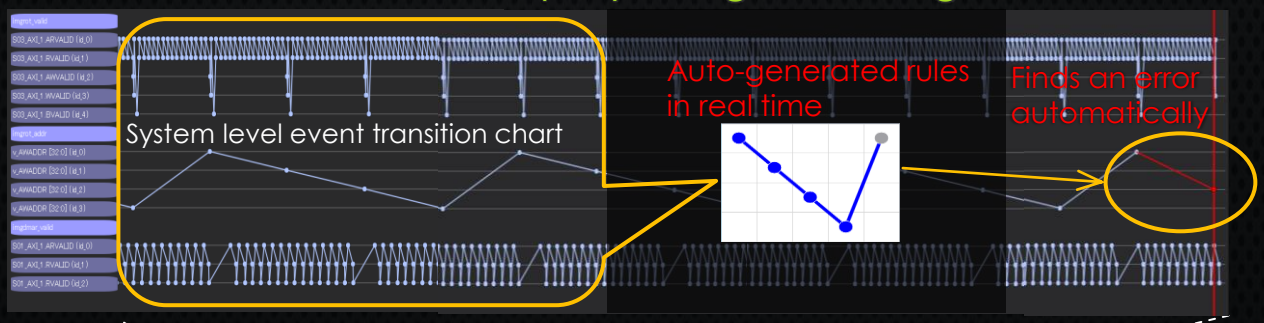
Debugging system-level failure takes long time



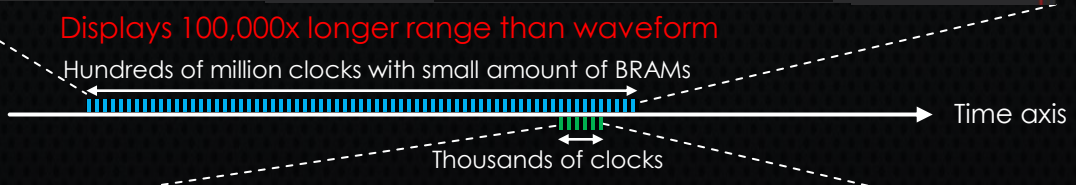


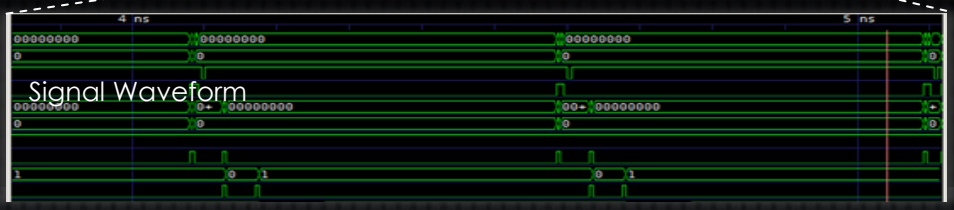
Needs user defined trigger conditions
Displays waveform in very narrow time range

VSTAR finds an error and displays long time range



Displays 100,000x longer range than waveform





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