# Michael Willett
# Texas Instruments, Software Systems Engineer

- 10 years in Physical Verification
  - CMOS Voltage Dependent Spacing DRC runset development and related Device Voltage checker
  - LVS runset development
- 8 years in Physical Architecture
  - IO Architecture Development and ESD protection implementation
  - STD Cell Architecture

# Insanity of DRC at 10nm

- Double / Triple patterning for each metal / via layer. Each metal layer needs 3 mask reticles designated by ‘colors’
- 3x rules to define spacing allowed for each color and proximity to other 2 colors
- 3x rules for metal interaction with adjoining Cont / Via layers
- What do you do when metal turns 90 degrees?
- Can colors be ‘stitched’ together?
- At what line width / space is coloring not required
- Are elevated voltages allowed for color layers?

# Insanity of Design at 10nm

- Designers need to have an understanding of the color dependency to know how to efficiently ‘fix’ DRC errors.
- Learning curve may become significant.
- Opportunities for smarter software techniques to display errors such that designers can make ‘smart’ corrections.
- What design / cycle-time trade-off should be employed that could simply the design flow but still permit enough entitlement?