

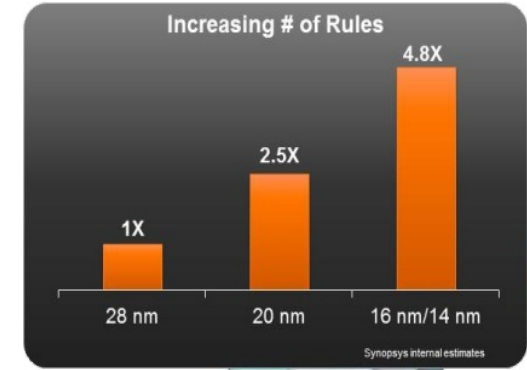
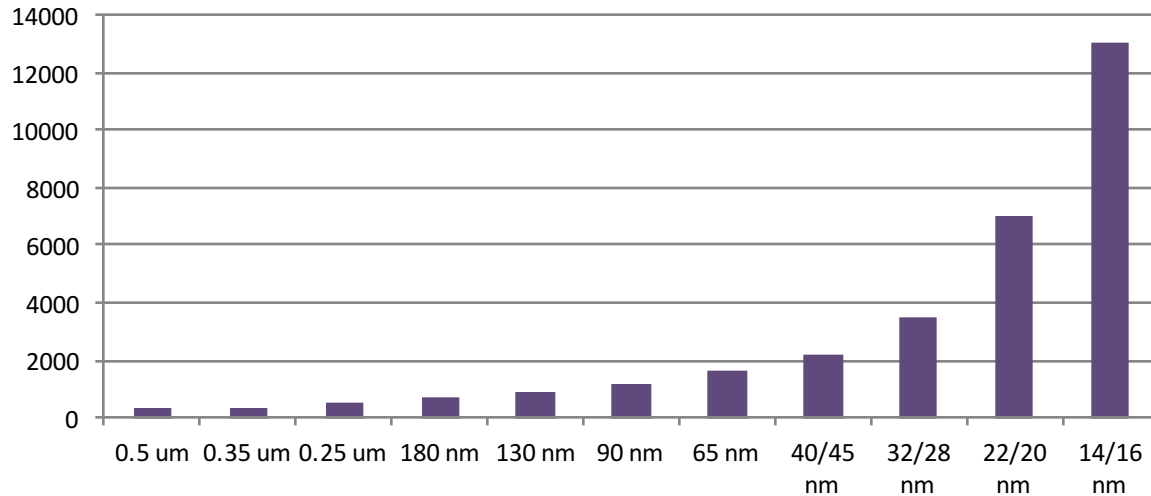
# THE INSANITY OF DRC RULES AND DFM AT 10NM AND BELOW

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*June, 2016*

# Number of Design Rules

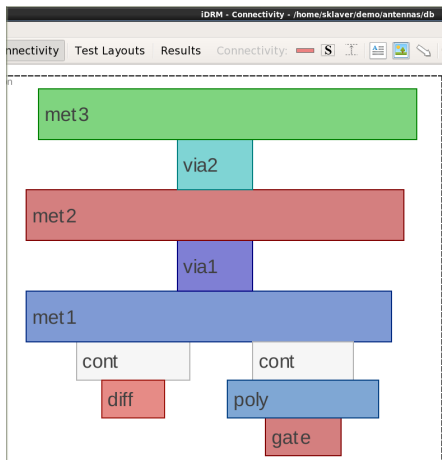
Number of design rules per technology node



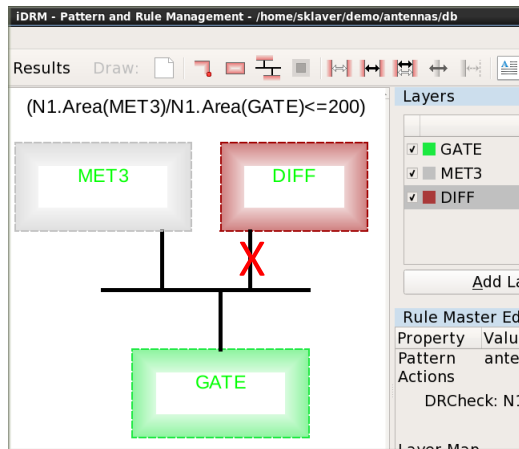
Source: Synopsys

- Overblown
- Administration of 10,000's rules is trivial
- Check parallelizes reasonably well, memory size has kept pace

# Design Rule Complexity



Layer stack



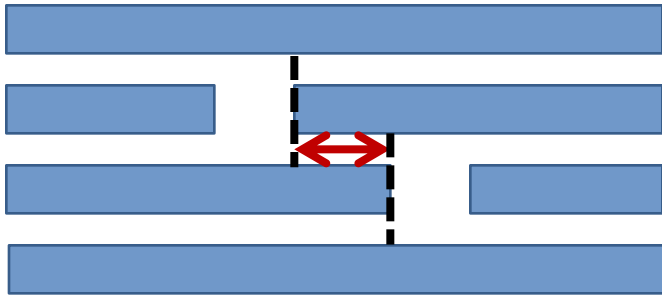
Design rule pattern

Design rule:

“Using the full layer stack, for all nets that are not connected to a diffusion, the ratio of (sum of area of met3) divided by (sum of area of gate) must be  $\leq 200$ ”

- Rules becoming less local, patterns
- Graphical / formal descriptions enhance clarity
- Ability to run a check of these descriptions is critical to develop a rule
- Executable spec, “check before deck” => instant feedback

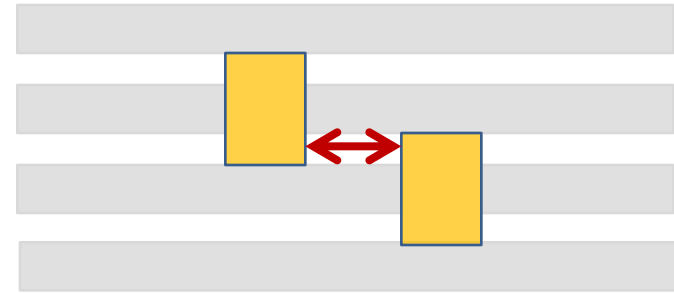
# Trading Design Rule Complexity



## Designer draws single layer

Rule:

“For adjacent horizontal wires, overlap of line-ends with length  $\geq 0.3u$  must be  $\geq 0.2u$ , or spacing must be at least  $0.2u$  “



## Designer draws two layers

Rule:

“Spacing between line-end cuts must be  $\geq 0.2u$ “