TOP TIP: COMPONENT PLACEMENT

CPU CONSTRUCTION AND IMPACT

In typical SBC (Single Board Computer) assembly, components with the highest power density are those which prove the most challenging to thermally manage. Restrictions around the space claim thermal engineers can use when interfacing with these devices mean that every opportunity must be used to mitigate the thermal resistance of your network between the device and the ambient world.

One such parameter within the control of the design team is the placement of the device itself on the board. As the board layout design develops, and real estate becomes more valuable, it becomes increasingly difficult for component positions to be adjusted and optimised for thermal solutions. It is imperative therefore that the designer have a firm grasp of the justifications of where a device goes from the very outset of product development.

Although there are many devices on an SBC that will require thermal attention, this article will focus primarily on CPUs as these typically post the high thermal power per square mm. A CPU's switching functionality is generated primarily within the cores of the device, seen clearly as six repetitive architectures on Figure 1, an Intel Coffee Lake Refresh chip.

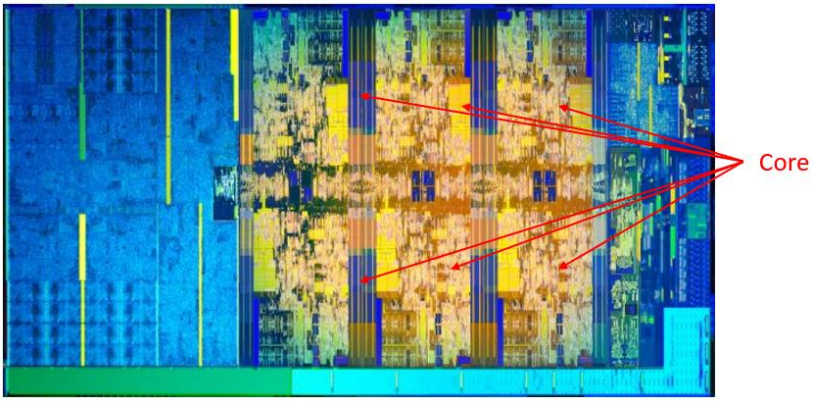


FIGURE 1 - DIE MAPPING OF INTEL 6 CORE ARCHITECTURE [1]

This local source of heat differs greatly to an FPGA or a GPU device, which can in turn accommodate significantly higher thermal design power figures. The justification for this will not be considered in this article, and has been included for reference purposes only.

Figure 2 shows an exploded diagram of a typical CPU device with the core locations highlighted as a red box within the Silicon Die. The relative size of the critical core location to the device itself provides a barrier to how well you can manage the ideal position of the thermal load.

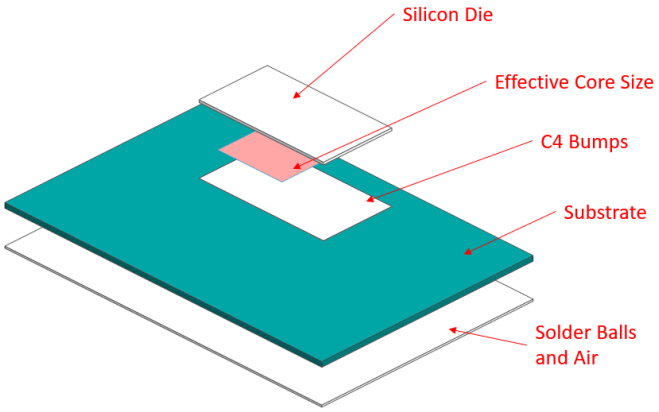


FIGURE 2 - EXPLODED VIEW OF A TYPICAL CPU CONSTRUCTION

A brief survey of existing 3U VPX cards that utilise this Intel architecture show varying approaches to component position. Figure 3 from Concurrent Technologies' TRE8x product utilises the CPU close to the lower edge of the board, while others align them more centrally.

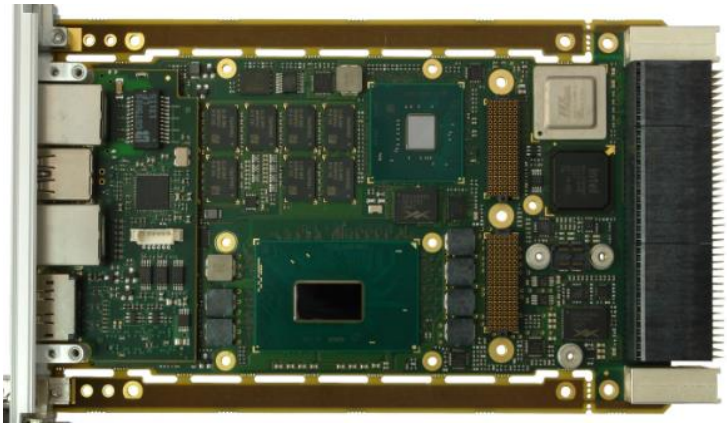


FIGURE 3 - TOP VIEW OF A 3U VPX SBC WITH COFFEE LAKE POSITIONED OFFSET FROM THE CENTRE [2]

Table 1 identifies a brief list of OEMs who have adopted the Intel Coffee Lake architecture into their product line. Data was not available for the exact position of these devices within the layout, but the position of these devices with respect to the centre and edge of the PCB can be clearly seen.

TABLE 1 - EXAMPLE PRODUCTS USING INTEL COFFEE LAKE REFRESH ARCHITECTURE IN DIFFERENT POSITIONS

PRODUCT NAME	OEM	CPU POSITION
TRE8X/MSD	Concurrent Technologies Plc	Offset
SBC3511	Abaco Systems	Central
SBC328	Abaco Systems	Central
C875	AiTech	Offset
VPX3-1260	Curtiss-Wright	Offset

THERMAL PRINCIPLES

Conductive heat transfer is fundamentally driven by Fourier's Law of Heat Conduction:

$$Q = kA\frac{\Delta T}{\Delta x}$$

Where *Q* is the thermal load (in Watts), *k* is the material conductivity (W/mK), *A* is the surface area (m^2), *ΔT* is the temperature drop (K) and *Δx* is the normal distance between the heat source and sink (m).

In embedded system design, *Q* and *ΔT* are typically fixed by the device selected for the board architecture and the ruggedization level of the product respectively.

Increasing *k* by replacing a typical Aluminium frame with Copper, or other more advanced materials, is a practical way of increasing your thermal capability and it typically the primary approach thermal engineers will use to combat the solution. While certainly effective this can have significant drawbacks such as weight and cost, major disadvantages for airborne or transport applications.

Material conductivity is also a contributing function of the area (*A*) as the improved properties allow the heat to spread faster within the heatsink, reducing the thermal flux density. Practically therefore it is almost impossible to define surface area in a 1D scenario such as this, where the heat source is significantly smaller than the cold wall, and more complex 3D methods should be employed.

The normal distance between heat source and the cold wall (*Δx*) carries equal power in this equation and yet is not always given consideration for each individual product release. While there are certainly restrictions on the position of a CPU, GPU or FPGA with respect to schematic design, and available real estate, optimising component position can be a very useful tool.

The thermal resistance is another used parameter to determine comparative performance of a system, defined as the temperature increase across a material per unit thermal power, and can be written:

$$R_{th} = \frac{\Delta T}{Q} = \frac{\Delta x}{kA}$$

R_{th} is a function of the thermal and geometric properties of the material in question and is useful for directly comparing similar design configurations. Note that as the distance between the heat source and sink is reduced (*Δx*), the resistance decreases.

Modern SBC and embedded system applications following VITA or IEEE conduction standards will produce very similar basic designs, promoting interoperability for system architects. Figure 4 below is

a typical 3U VPX application with a CPU position shown for reference only (not intended to be representative of actual product).

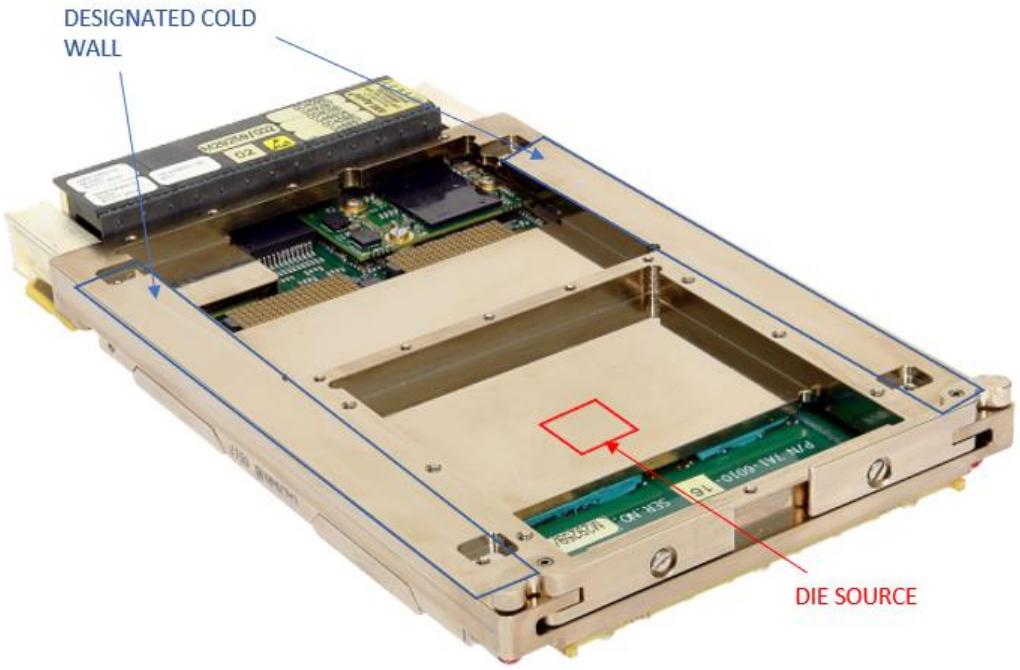
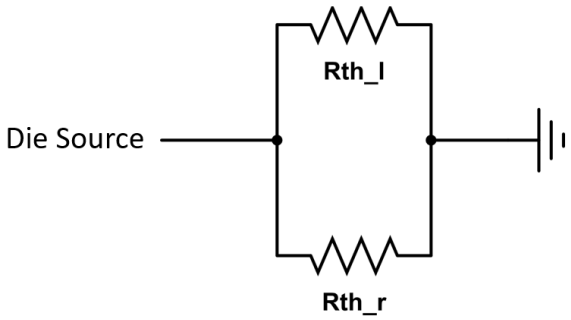


FIGURE 4 - VPX APPLICATION WITH HEAT SOURCE AND SINKS [3]

In this application, heat from the die has two options to travel to the heatsink; the left and the right cold wall. This can be represented as a parallel resistance network:



And can be calculated as follows:

$$\frac{1}{R_{system}} = \frac{1}{R_{th\_l}} + \frac{1}{R_{th\_r}}$$

In a simplistic scenario, both the area and conductivity of the heatsink is consistent and equal between the cold walls. Therefore, when the die is centrally located the right resistance is equal to the left, simplifying the equation further:

$$R_{system} = \frac{R_{th}}{2} = 0.5R_{th}$$

If the die were moved either side of central, this would proportionally change the respective resistances to suit. If the die was moved halfway closer to one edge, so $R_{th\_r}=R_{th}/2$ and $R_{th\_l}=3R_{th}/2$, then Equation 3 equates to:

$$\frac{1}{R_{system}} = \frac{1}{\frac{3R_{th}}{2}} + \frac{1}{\frac{R_{th}}{2}} = \frac{8}{3R_{th}}$$

And,

$$R_{system} = \frac{3R_{th}}{8} = 0.375R_{th}$$

In 1D theory, moving the position of the die away from perfectly centre therefore should have a positive impact on the network resistance and so the performance of each product should be improved.

THE IMPACT OF XMC SITES

Evaluating Fourier's Law of Conduction further we can consider the impact of cross sectional area in this study. The amount of heatsink material available to carry heat is greatly affected by the presence of an Express Mezzanine Card (XMC). The component keep out areas for these cards require considerable amounts of material to be removed directly above the thermal load, clearly visible in Figure 5.

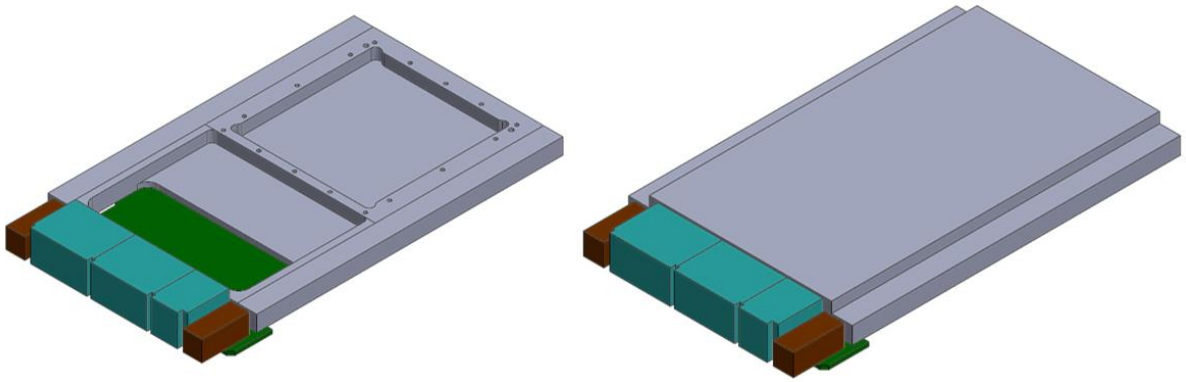


FIGURE 5 - MODEL OF A 3U CARD WITH AND WITHOUT AN XMC SITE

These XMC sites are also given an option for the inclusion of secondary thermal interface mountings close to the cold walls, see Figure 6 and Figure 7.

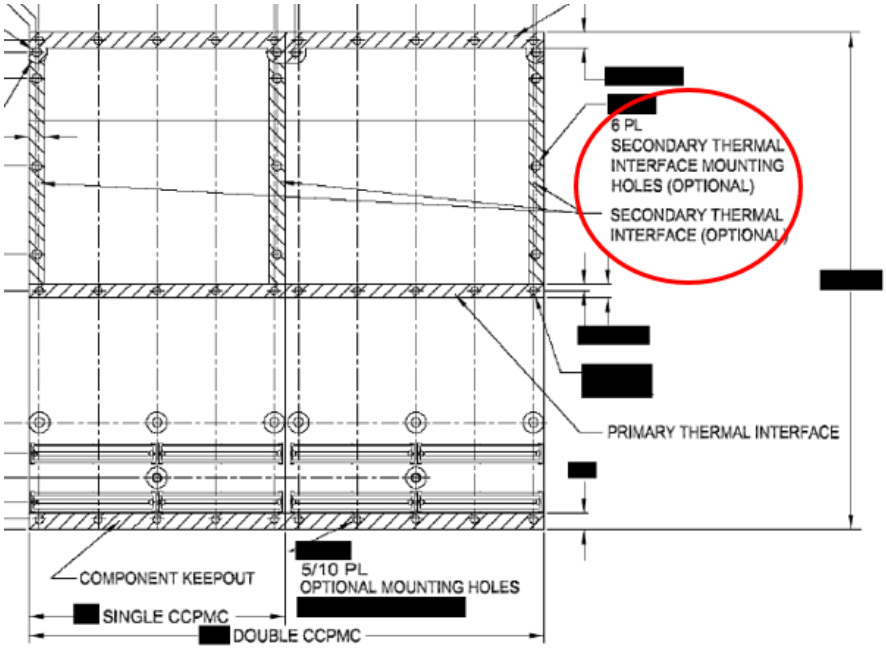


FIGURE 6 - VITA SPECIFICATION IDENTIFYING THE OPTIONAL SECONDARY THERMAL MOUNTING HOLES [4]

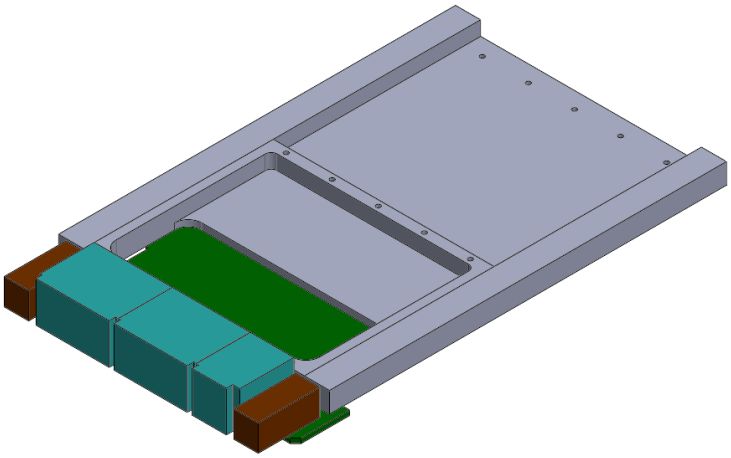


FIGURE 7 - MODEL OF A 3U CARD WITH SECONDARY THERMAL INTERFACE BARS REMOVED

It is expected that removal of material for the XMC will have a significant impact on the power that can be carried by the system as it will restrict the area (*A*) available for heat to pass through. While some of this loss of area may be recovered by moving the device underneath the secondary thermal interface area, the impact of making this section removable will be considered for completeness.

Running a simple thermal simulation with a single device board can provide a good comparative study of the direct impact of moving your prime thermally critical device and in what configurations this provides the greatest thermal benefit.

For the purposes of this study contact between the device and the board has been simplified, although gives a realistic representation of a good thermal assembly. Unless otherwise stated, all parameters within these simulations are kept constant.

The key variable in this investigation is to understand the impact of CPU placement on a small form factor card. Considering the observations made earlier in this report from competitive product layouts, the two options that will be compared are shown below:

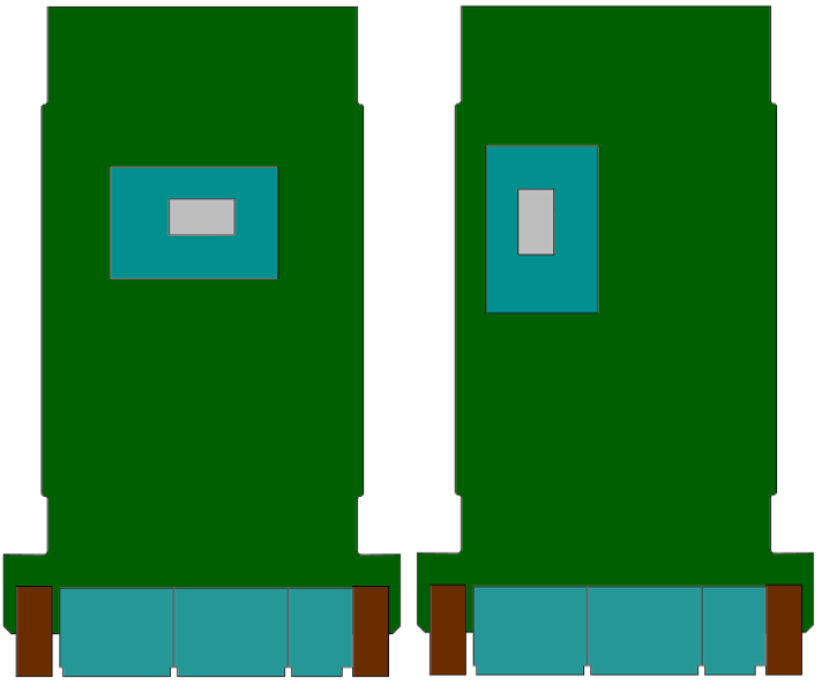


FIGURE 8 - COMPARATIVE POSITIONS OF CPU UNDER TEST

The positions are selected such that:

A. the Die Source is aligned geometrically centrally in the board
B. the Die Source is pushed 70% to one side of the board, with the die rotated 90° to allow for more extreme alignment.

Each of these configurations will be simulated individually to determine how component position impacts performance in a range of product options:

TABLE 2 - SIMULATION CONFIGURATION TABLE

Simulation #	Configuration
1	No XMC requirement
2	XMC requirement, embedded interface bars
3	XMC requirement, removable interface bars
4	XMC requirement, no interface bars

Figure 9 shows these configurations graphically. Scenario #3 is geometrically similar to scenario #2, however the thermal loss that would be experienced across a dry aluminium contact (seen with removable interface bars) is included in the simulation in the form of a high contact resistance.

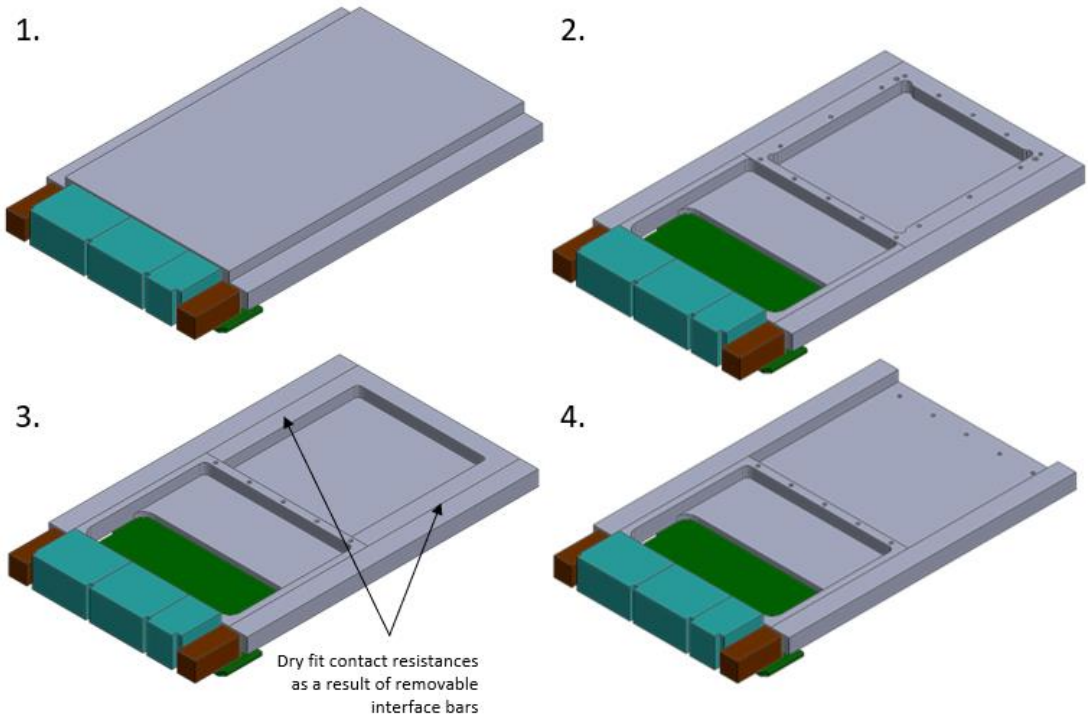


FIGURE 9 - GRAPHICAL REPRESENTATION OF HEATSINK CONFIGURATIONS UNDER TEST

RESULTS

Table 3 shows the resultant impact on junction temperature for each configuration. A positive Delta value indicates that the temperature of the chip has **decreased** in the offset position, and a negative value indicates that the temperature has **increased**.

TABLE 3 - SIMULATION RESULTS SHOWING THE IMPACT OF MOVING THE CPU POSITION

Simulation #	Delta (°C)
1	0.56
2	5.64
3	3.49
4	3.14

As predicted by the resistance network calculations given above, when the cross-sectional area is kept constant (scenario #1) a die offset has a small beneficial impact on the performance of the device. While the absolute effect of die temperature cannot be compared linearly to these 1D equations, this gives confidence that the simulation, and therefore practical application, is producing logical results.

Scenario #2 shows the largest contrast in heatsink thickness' between the two locations, and as a result it shows the greatest performance distinction.

Scenario #3 and #4 show very similar results which indicates that loss across the dry fit connection is high, which is unsurprising given the criticality of Thermal Interface Materials in electronics cooling.

For an embedded thermal engineer, the 3°C temperature gain in configuration 3 and 4 is a significant performance enhancement. For most MilAero plug-in modules, the VITA defined environmental specifications determine the ruggedization levels to which the product must perform. For conduction cooled units, the maximum cold wall (see Figure 4) temperature for these units is +85°C [5]. As silicon transistor performance degrades with temperature, most performance CPUs have a safety cut-off limit at 100°C for the junction (die source) [6], preventing permanent damage from long term exposure to high temperature.

Considering the 15°C temperature range available, a 3°C drop accounts for a significant 20% of the thermal budget.

CONCLUSION

This article shows that the impact of an XMC site on a product has a drastic impact on the effectiveness of component position. While in theory the proximity of a high power component to one cold wall should have noticeable positive impact to the performance of the device, the available cross section above the device for heat transfer has a much larger influence. The requirement for a mezzanine card should be known at a very early stage in product development and is an important factor in determining the optimal device position.

It should be noted that the findings in this report are based on theoretical principles only and will not reflect the performance or accuracy of any active products referenced herein. This should be used as an educational article only and was written with no knowledge of the actual performance of any products identified.

These products are identified for their positional diversity only, with many contributing factors ignored for the purpose of the study. Each solution is bespoke to the product use-case and should be managed as such.

APPENDIX

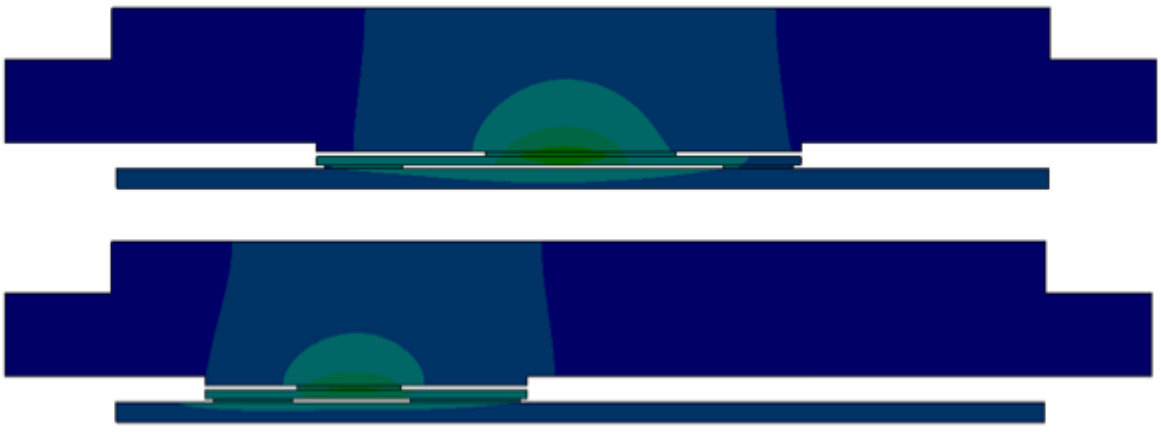


FIGURE 10 - A THERMAL PLOT THROUGH THE DIE JUNCTION IDENTIFYING THE SIMILAR DISPERSION OF FLUX IN A SOLID HEATSINK

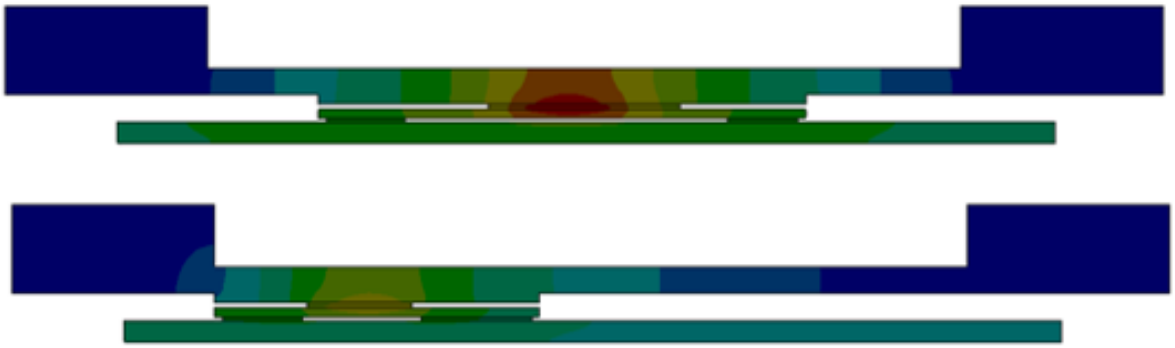


FIGURE 11 - A THERMAL PLOT THROUGH THE DIE JUNCTION IDENTIFYING THE DISTINCTLY DIFFERENT DISPERION OF FLUX IN AN XMC CAPABLE HEATSINK

REFERENCES

[1] ExtremeTech, “Intel’s Coffee Lake Refresh Offers Up to 6 Cores, Goes On Sale Oct. 5,” [Online]. Available: https://www.extremetech.com/computing/256378-intels-coffee-lake-refresh-offers-six-cores-goes-sale-october-5.

[2] Concurrent Technologies Plc, “TR E8x/msd – 3U VPX Processor,” Concurrent Technologies Plc, [Online]. Available: https://www.gocct.com/product/tr-e8x-msd-vpx-processor/.

[3] Concurrent Technologies Plc, “TR E5x/3sd-RCx – Rugged VPX Processor,” 2020. [Online]. Available: https://www.gocct.com/product/tr-e5xmsd-rc-rugged-vpx-processor/.

[4] VITA, “ANSI/VITA 20-2005 for Conduction Cooled PMC,” VITA - VMEBus International Trade Association, 2018.

[5] VITA, “ANSI/VITA 47.0-2019,” VITA, 2019.

[6] Intel, *Intel Coffee and Whiskey Lake Mobile Platform Thermal Mechanical Design Guide,* Intel, 2020.