DID YOU KNOW? TOP CAN MEAN BOTTOM

Electronic device developers have created and utilised common notations for calculating the thermal cooling needs of their component. Typical examples of this include: Junction-to-Ambient (θ_{JA}), Junction-to-Board (θ_{JB}) and Junction-to-Case (θ_{JC}) resistance. These metrics allow users to reliably determine the operating conditions of their devices, and in turn design suitable cooling methods to ensure operating life is maximised. For a higher performance device, which requires an external thermal solution, θ_{JC} is the most appropriate of these metrics. It allows for a direct sizing of a heatsink to reduce the impedance between the top of the device and ambient.

9.2 THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (no airflow)		26.8		°C/W
θ_{JB}	Junction-to-board thermal resistance		16.2		
θ_{JC}	Junction-to-case thermal resistance		40		

FIGURE 1 - AN EXAMPLE OF THE 3 PRINCIPLE THERMAL RESISTANCE METRICS USED IN ELECTRONICS COOLING MANAGEMENT [1]

Sounds simple enough?

Unfortunately, while the term θ_{JC} has been standardised within the JEDEC publications, the definition of case remains relatively undefined. These standards state only that θ_{JC} is, “the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface [2].”

Different component vendors will have different interpretations of where this case temperature is measured, depending on the device construction. Some packages have mechanisms such as heat slugs or exposed pads to remove heat from the top, bottom, or both surfaces of the package. When only a single surface is used for heat removal, this is the surface that would be used for θ_{JC} based on the definition given above [3].

In many situations, typically VME/VPX embedded SBCs, the only possible thermal solution is from the top of the device. Taking the example of a component with a heat slug soldered to the PCB (bottom facing), it would therefore be in inaccurate to size the correct solution using θ_{JC} given that the heatsink will be mounted on the top.

This has given rise to two variants of the same metric, $\theta_{JC\,(top)}$ and $\theta_{JC\,(bottom)}$, which the vendor should identify. The difference between the two is not always defined causing confusion for developers. In this scenario, top always refers to the surface facing away from the PCB, and bottom is the surface of the package facing toward the PCB.

CASE STUDY

The two components in this study have a number of similarities: both are SATA redrivers, have QFN packaging, have the same footprint and both utilise a thermal ground pad.

Component A: Texas Instrument SN75LVCP601 [4]

Component B: Maxim Integrated MAX14970 [5]

Device drawings can be seen in the Appendix attached at the end of this document.

It would be reasonable to expect similar thermal characteristics for both devices considering their similar structure. Figure 2 and Figure 3 below have been taken from the respective component datasheets, and show the significant difference that labelling case can make.

6.4 Thermal Information

THERMAL METRIC[1]		SN75LVCP601 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10	°C/W

FIGURE 2 - THERMAL INFORMATION FOR TI SATA REDRIVER

Package Thermal Characteristics (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 6°C/W

FIGURE 3 - THERMAL INFORMATION FOR MAXIM SATA REDRIVER

Note that the junction-to-ambient resistance, θ_{JA} for both devices is very similar – confirming a similar package construction – however the θ_{JC} of the Maxim device is 85% lower than that sold by TI. While both definitions are technically correct, it allows for misinterpretation of figures and therefore potentially wayward thermal estimates.

In short, care should always be taken by the user to consider the intent of the author when using these metrics.

REFERENCES

[1] Texas Instruments, “Industrial Temp, Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver,” December 2009. [Online]. Available: https://www.ti.com/lit/ds/slls931b/slls931b.pdf.

[2] JEDEC, “EIA/JESD51-1 Integrated Circuits Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device),” December 1995. [Online]. Available: https://www.jedec.org/sites/default/files/docs/jesd51-1.pdf.

[3] Texas Instruments, “Semiconductor and IC Package Thermal Metrics,” April 2016. [Online]. Available: https://www.ti.com/lit/an/spra953c/spra953c.pdf.

Appendix A

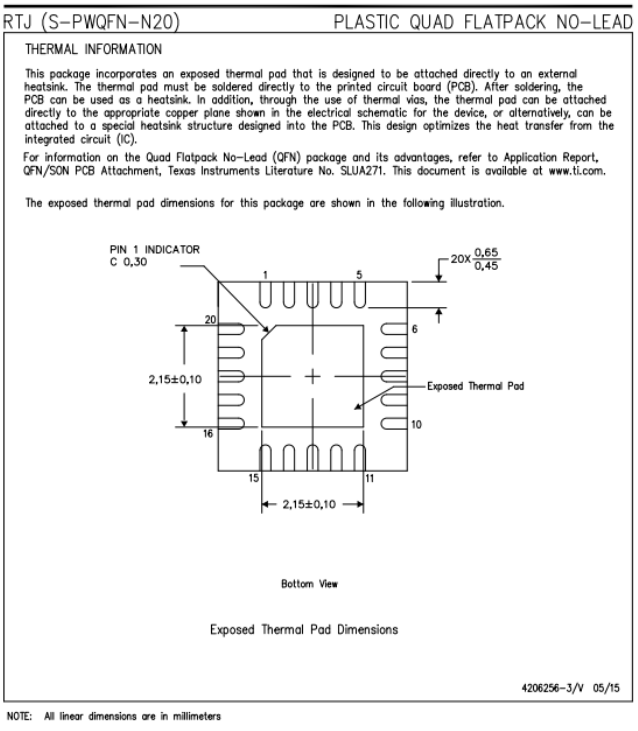

FIGURE 4 - DEVICE DRAWING OF TI SATA REDRIVER [4]

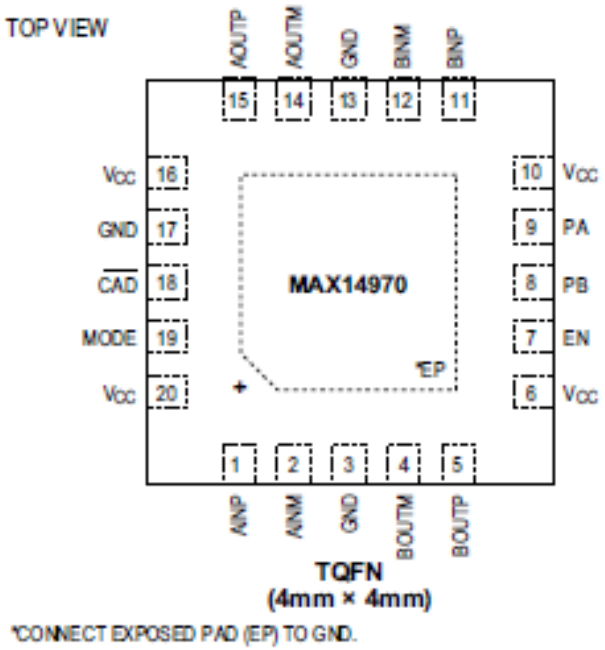

FIGURE 5 - DEVICE DRAWING OF MAXIM SATA REDRIVER [5]