
SIMERA

SENSE

HyperScape100

Datasheet

Document Number: 036552
Author(s): G. Dreijer
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List of Abbreviations

Abbreviation	Description
A	Ampère
ADC	Analog to Digital Converter
BOL	Beginning of Life
°C	Degree Celsius
CAN	Controller Area Network
CCD	Charge Coupled Device
CE	Control Electronics
CMOS	Complementary Metal Oxide Semiconductor
CSKB	CubeSat Kit Bus
DC	Direct Current
FPGA	Field Programmable Gate Array
FEE	Front-End Electronics
FWHM	Full Width at Half Maximum
GND	Ground
g_{rms}	Gravitation Constant, Root Mean Square ($g = 9.81 \text{ m/s}^2$)
GPIO	General Purpose Input Output
GSD	Ground Sampling Distance
HPP	Half Power Point
Hz	Hertz
I ² C	Inter-Integrated Circuit
I/O	Input / Output
kg	Kilogram
kHz	Kilohertz
km	Kilometre
krad	Kilorad
LEO	Low Earth Orbit
lp	Line Pairs
LVDS	Low Voltage Differential Signalling
mA	Milliampere
MHz	Megahertz
mm	Millimetre
ms	Milliseconds
nm	Nanometre
OFE	Optical Front-End
PCB	Printed Circuit Board
SDR	Single Data Rate
SEL	Single Event Latch-up
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SU	Sensor Unit

Abbreviation	Description
TDI	Time Delay Integration
TID	Total Ionising Dose
U	Unit (CubeSat)
µm	Micrometre
V	Volt
VNIR	Visible and Near-Infrared
W	Watt

1. Overview

The HyperScape100 is a hyperspectral push-broom imager primarily designed for earth observation applications as a payload for CubeSat satellites. It is based on 12.6-megapixel image sensor and continuously variable filter in the visible and near-infrared (VNIR) spectral range. The HyperScape100 provides continuous line-scan imaging in up to 32 spectral bands, each with digital time delay integration (TDI).

The optical front-end (OFE) has a large aperture diameter and long focal length within a compact form factor, resulting in a ground sampling distance (GSD) of 4.75 m at an orbital height of 500 km. The modified Cassegrain optical design brings performance to the edge of the object field over the whole spectral range at an ultra-low distortion. The HyperScape100 is engineered to withstand the rigours of the space environment and maintain performance across a wide temperature range. Its compact form factor is optimised for integration into 3U or larger CubeSat structures.

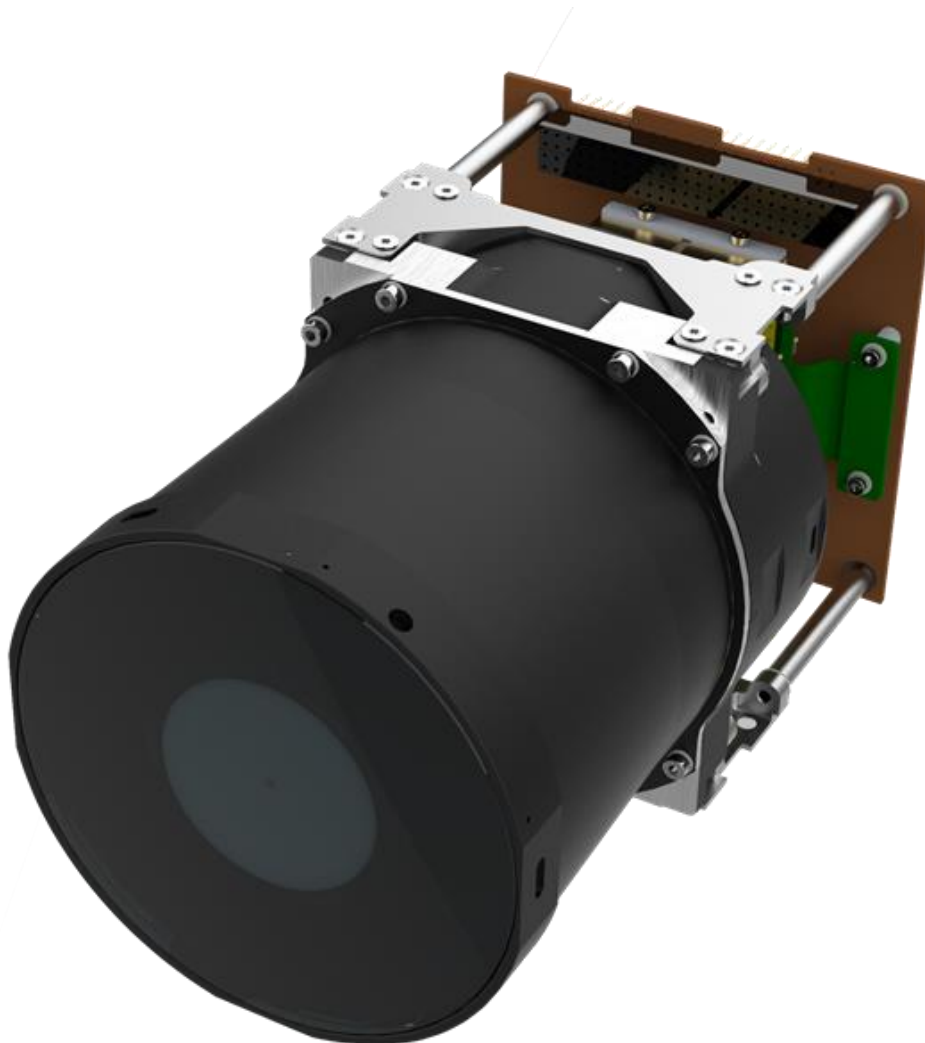


Figure 1-1: HyperScape100 Imager

1.1 Features

- 4.75 m GSD (at 500 km orbit height)
- The swath of 19.4 km (at 500 km orbit height)
- Up to 32 spectral bands in the VNIR range
- FWHM bandwidth of 4% of the central wavelength
- 128 Gigabyte non-volatile storage capacity for up to 3900 km strip (at 500 km orbit height)
- On-board image processing and compression (optional)
- Comprehensive onboard telemetry and health monitoring
- Environmental verification based on GSFC-STD-7000

1.2 Applications

- Precision agriculture
- Forestry and land use
- Energy and infrastructure
- Coastal monitoring
- Air quality

1.3 Key Specifications

Table 1-1: Key Specifications

Optics	
Focal Length	580 mm ±1 mm
Aperture	95 mm
Full Field of View	2.22° (Across Track)
Imaging	
Configuration	Line-scan (push broom)
Sensor Technology	CMOS
Cross Track	4096 pixels
Pixel Size	5.5 µm
Pixel Depth	10-bit
Spectral Bands	Up to 32
TDI Stages	Up to 32 per band (user assigned)
Line Rate	Up to 2600 Hz ⁽¹⁾
Spectral Range	487 nm – 790 nm (filter option 1) 502 nm – 801 nm (filter option 2) 516 nm – 810 nm (filter option 3)
Spectral Band Width	FWHM: ~4% of the central wavelength
Transmittance	51% (at 550 nm) ⁽²⁾
On-Board Electronics	
Storage Capacity	128 Gigabyte NAND Flash
Continuous Strip Length	Up to 800 km ⁽³⁾
Image Processing	Binning, Thumbnails
Image Compression	Lossy/Lossless (optional)
Control Interface	I ² C or SPI CAN, RS-422 (optional) Customer specific interface (optional)
Data Interface	LVDS (or customer specific interface, optional)
Power Supply	5 V DC
Power Consumption	< 6 W (during imaging mode)
Mechanical	
Mass	1.2 kg
Dimensions	98 x 98 x 176 mm
Environmental	
Operating Temperature	-10 to +50 °C
Radiation (TID)	> 15 krad

(1) Dependant on orbit height, see Figure 3-1

(2) Including filter

(3) At 500 km orbit height

1.4 Functional Components

The HyperScape100 imager consists of the following functional components:

- **Optical Front-End (OFE):** The xScape100 VNIR OFE is used to focus the incoming light onto the focal plane.
- **Sensor Unit (SU):** It consists of the CMOS sensor front-end electronics (FEE) and a continuously variable filter. It also includes the sensor plate mechanics which allows it to be mounted at the OFE's focal plane.
- **Control Electronics (CE):** The CE provides control and data interfaces to the satellite bus. It performs sensor control, data handling, data storage, and image processing. It is also responsible for power regulation and management, as well as health monitoring and telemetry.

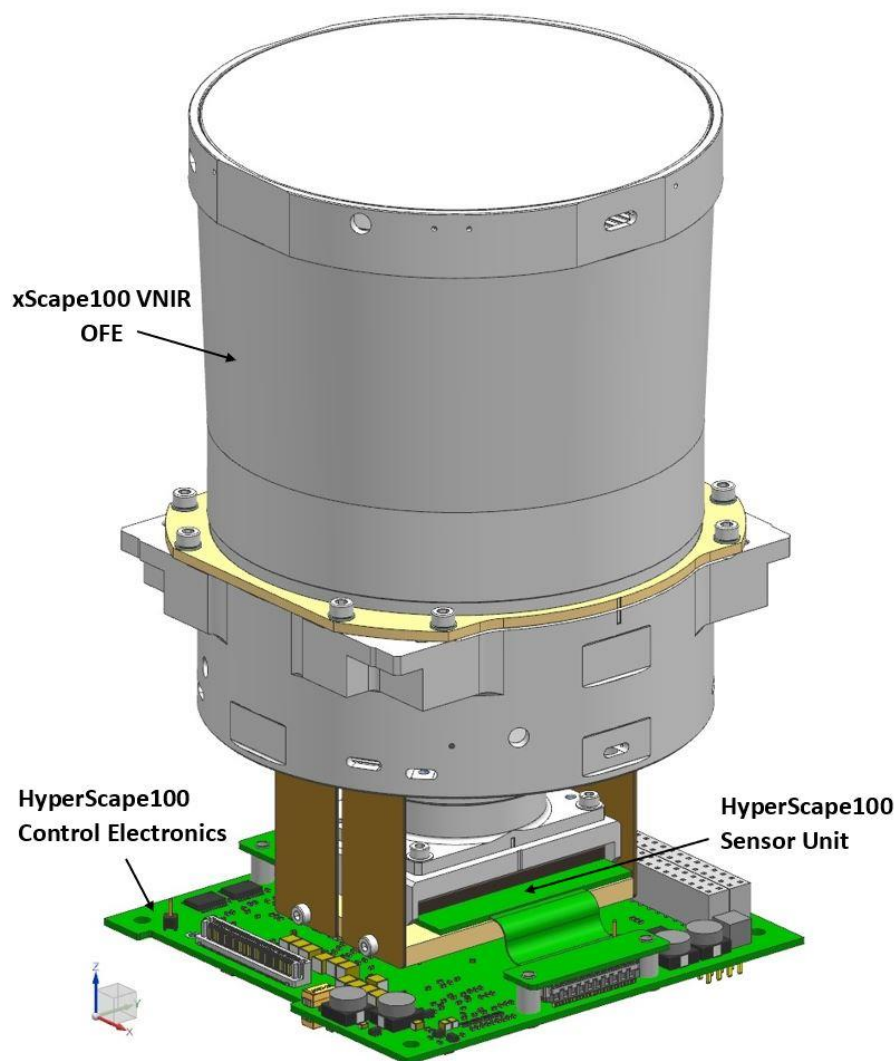


Figure 1-2: HyperScape100 Functional Components

2. Detailed Description – Optical Front-End

The xScape100 VNIR OFE is used as an optical front-end for the HyperScape100. Following the unique demands of space-based imaging payloads, the xScape100 VNIR OFE was designed to accommodate a wide spectral range, be robust and maintain performance across a wide temperature range. The optical design of the imaging payload incorporates a modified Cassegrain optical design with a meniscus entrance lens which defines the entrance pupil of the payload and adds additional environmental protection to the OFE during integration, launches and in operation.

Table 2-1: OFE Characteristics

Description	Value
Focal Length	580 mm ± 1 mm
F-Number	6.1
Front Aperture Diameter	95 mm
Obscuration Diameter	47.2 mm
Distortion	< 0.165%
On-Axis MTF	18% at Nyquist (93 lp/mm)

For further information, see the xScape100 VNIR OFE Datasheet.

3. Detailed Description – HyperScape100 Sensor Unit

The HyperScape100 Sensor Unit houses the Front-End Electronics (FEE) which is based on a 12.6-megapixel CMOS sensor. The sensor is fitted with a continuously variable filter, and three standard spectral range selections are available, as shown in Table 3-1. The out-of-band transmittance of the filter is less than 0.01%.

Table 3-1: Filter Range Options

Filter	Spectral Range
Option 1	487 nm – 790 nm
Option 2	502 nm – 801 nm
Option 3	516 nm – 810 nm

The windowing mode of the sensor allows the capturing of up to 32 user-selectable spectral bands. The bandwidth of each band is approximately 4% of the centre wavelength. This results in the FWHM increasing from 19.4 nm at 487 nm to 32.4 nm at 810 nm. The centre wavelength of each band can be selected in steps of 0.4 nm. The nature of the continuously variable filter means that the TDI stages applied to each band influence not only the signal-to-noise ratio (SNR) but also the bandwidth. Fortunately, the increase in bandwidth for a typical number of TDI stages is very small. Even with 16 TDI stages, the effective increase in bandwidth is less than 8%, as shown in table Table 3-2.

Table 3-2: Spectral Band Examples

Centre Wavelength (nm)	TDI Stages	FWHM Bandwidth (nm)	SNR
487	1	19.4	14.9
487	8	20.2	42.3
487	16	21.0	59.9
810	1	32.4	24.2
810	8	33.1	68.4
810	16	33.9	96.7

The number of TDI stages for each band may be individually selected by the user in multiples of 2, to a maximum of 32. The sum of all the TDI stages (across all the bands) is limited by the line scan rate, which is determined by the orbit height for earth observation satellites, as shown in Figure 3-1. The graph clearly shows that at lower orbit heights, an increased line scan rate reduces the total number of TDI stages available. For example, at 500 km orbit height, a total of 320 TDI stages are available so that the user may select 10 TDI stages for each of the 32 bands.

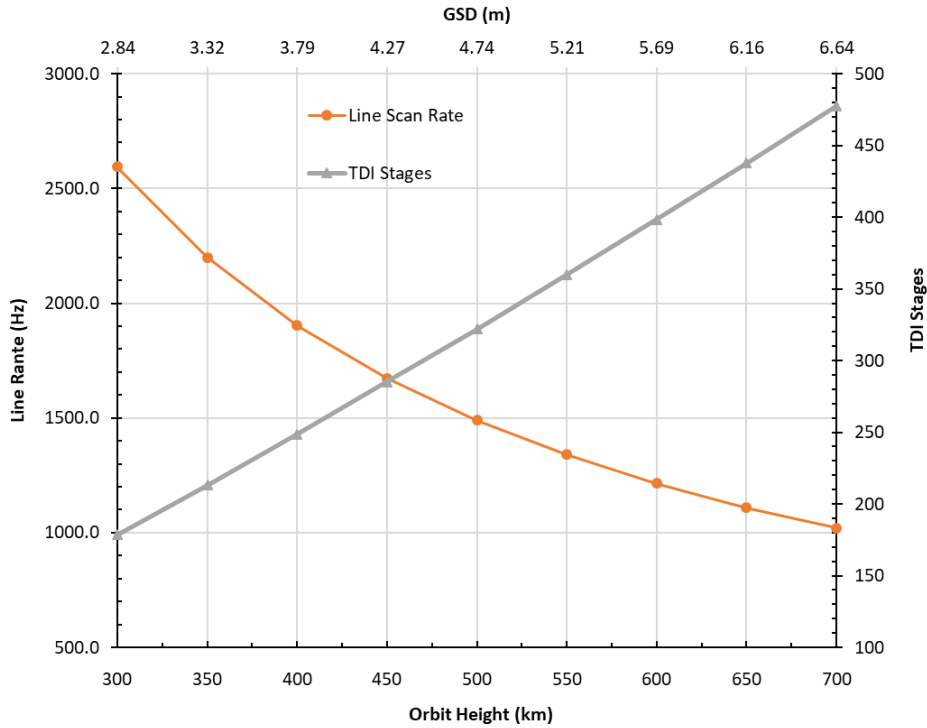


Figure 3-1: Line Rate and TDI Stages

The signal-to-noise ratio with a selection of TDI stages, at an orbit height of 500 km is shown in Figure 3-2. A radiance level of $100 \text{ W}\cdot\text{m}^{-2}\cdot\text{sr}^{-1}\cdot\mu\text{m}^{-1}$ is assumed across the spectral range for all of the SNR values.

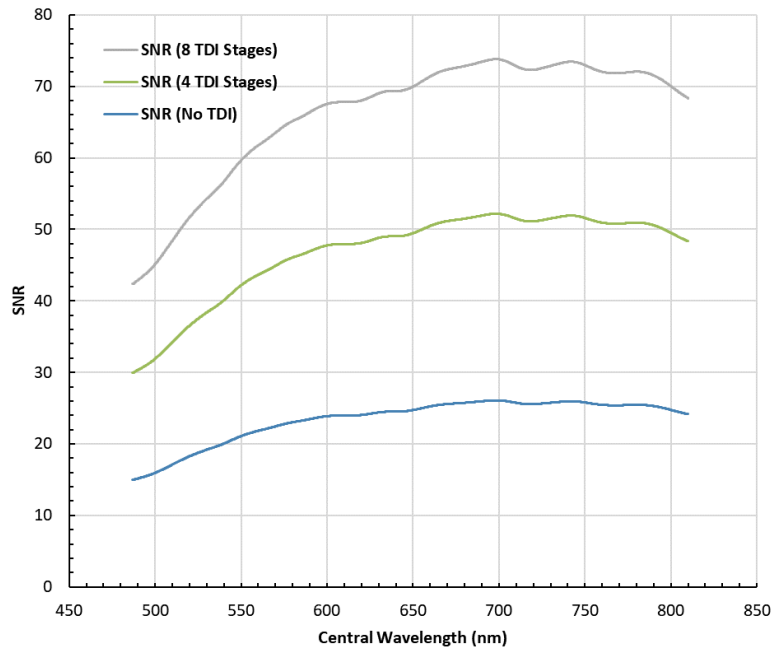


Figure 3-2: SNR vs Central Wavelength

4. Detailed Description – Control Electronics

The Control Electronics (CE) is a single PCB with a standard PC-104 form factor. It interfaces to the Front-End Electronics (FEE) of the HyperScape100 Sensor Unit as well as the external satellite bus. The functionality of the CE is largely based on a high-performance FPGA, which allows image data to be captured at high data rates, processed on-board, and delivered via a high-speed interface. The CE is highly configurable, with several standard selections and options available, which allows for flexible integration into existing systems.

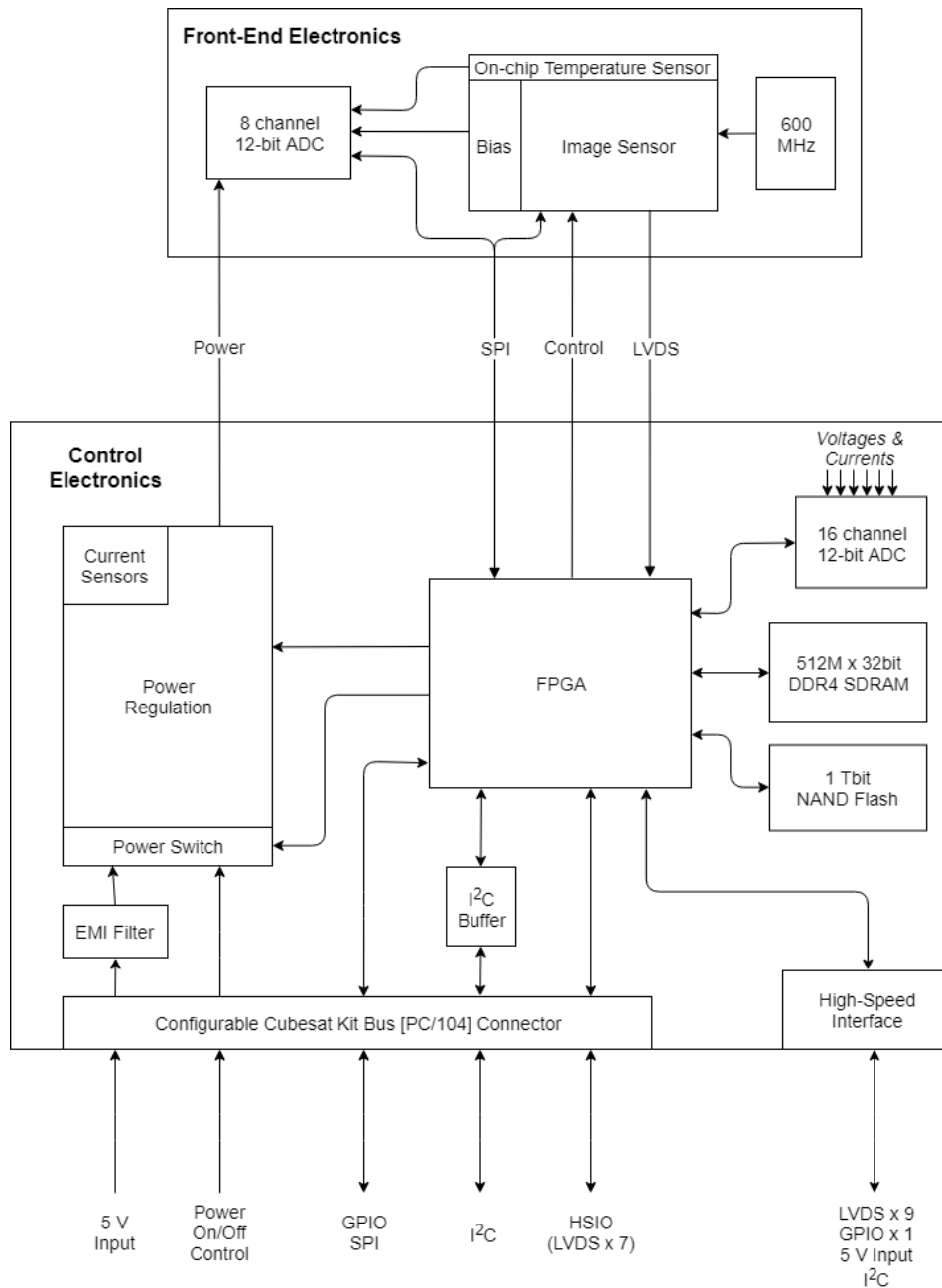


Figure 4-1: Control Electronics Block Diagram

4.1 Power Supply

The CE requires a direct current (DC) power supply regulated at 5 V ± 10% with a current rating of at least 1.5 A. Typically, the satellite bus supplies a switched power supply to the CE. In cases where the power supplied to the CE is not switched, user control of an on-board power switch is available. The CE monitors the current consumption of various sub-circuits and can initiate a full power-down or power-cycle if an over-current event occurs. This serves to protect against radiation-induced single-event latch-up (SEL). The different power switching possibilities are shown in Table 4-1

Table 4-1: Power Switching Alternatives

Power Mode	Description	Over-current
Bus Switched	External 5 V supply is switched.	Power-cycle
User-Controlled Switch (Direct)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Power Control line is driven low	Power-cycle
User-Controlled Switch (Latched)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Control command to CE	Power-cycle or Power-down ⁽¹⁾

(1) Drive the Power Control line low for over-current power-down, or high for power-cycle.

4.2 Control Interface

The CE implements an I²C slave which is used as a control interface for commands and telemetry. It supports standard-mode (100 kHz) and fast-mode (400 kHz), as well as 3.3 V or 5 V signal levels. The 7-bit slave address is configurable, as well as the optional pull-up resistors.

The CE also provides a Serial-Peripheral Interface (SPI), which may be accessed via any available GPIO pins (see section 4.4). Also, the control electronics includes dedicated transceivers on-board to make provision for options such as a CAN interface or an RS4-22/RS-485 interface.

Table 4-2: Control Interface Options

Interface	Details
I ² C	Standard
SPI	Standard
CAN	Optional
RS-422/RS-485	Optional
Customer Specific Interface	Optional

4.3 High-Speed Interface

The High-Speed Interface is used for dedicated high-speed transfers, where image data is read out to a payload processor or downlink transmitter. The interface uses an in-house streaming protocol and five LVDS pairs to provide a data output with a bit rate of up to 200 Mbit/s, as shown in Table 4-4.

Table 4-3: High-Speed Data Interface Characteristics

Characteristic	Value
LVDS Pairs	4 or 5 ⁽¹⁾
Clock Frequency	100 MHz
Data Alignment	Centred
Data Lanes	2
Data Lane Rate	SDR

(1) 4 LVDS pairs excluding flow control, 5 pairs including flow control.

The 100 MHz source-synchronous clock is centre aligned to the two single data rate (SDR) data lanes. The data lanes are synchronised to the free-running clock using a dedicated synchronisation signal. Optional flow control is also available in cases where the receiver needs to throttle the incoming data stream. Table 4-4 describes the role of the LVDS pairs in more detail. The details pin assignment of the interface is shown in section 5.2.

Table 4-4: High-Speed LVDS Description

Signal Name	Description	Direction
Clock	Clock	Output
Sync	Synchronisation	Output
D0	Data Lane 0	Output
D1	Data Lane 1	Output
RR	Flow Control (Receiver Ready)	Input

4.4 General Purpose and High-Speed Digital I/Os

The CE includes a total of 30 I/O lines at a 3.3 V signal level, which may be used as part of the standard configuration or customer-specific interfaces (optional). These are essentially pins that are directly connected to the FPGA. All of these I/Os may be configured as single-ended general-purpose I/Os (GPIOs), while select I/Os maybe be configured as LVDS (differential) pairs for use as High-Speed I/Os (HSIOs). A total of 7 LVDS pairs are available to allow for customer-specific interfaces to be implemented. The available I/Os are summarised in Table 4-5. They are all located on the PC-104 connectors, with pin assignments described in 5.1.

Table 4-5: GPIOs and HSIOs

Description	Number
Total I/Os	30
GPIOs	Up to 30 ⁽¹⁾
HSIOs (LVDS pairs)	7

(1) The number of GPIOs available is reduced by 2 for each HSIO pair used.

When the SPI interface is selected, 4 GPIO lines must be reserved for this interface. GPIOs are also typically used as outputs to indicate a specific status or event (optional).

4.5 Telemetry and Health Monitoring

The CE provides comprehensive telemetry and health monitoring, with 32 unique measurement channels available, as shown in Table 4-6. The health monitoring allows for thorough analysis and fault-detection of the electronics while in-flight.

Table 4-6: Telemetry Measurement Channels

Sub-Circuit	Channel Description	Number of Channels
FEE	Supply Voltages	2
	Bias Voltages	8
	Sensor Temperature	1
CE Power Regulation	Supply Voltages	10
	Supply Currents	7
CE FPGA	Chip Temperature	1
	Supply Voltages	3
TOTAL		32

5. Electrical Interfaces

The HyperScape100 Control Electronics features two connectors for external interfacing – a standard CubeSat Kit Bus (CSKB) PC-104 connector pair (H1 and H2) and a custom high-density connector (P5) for high-speed data transfers. The pin assignment of the PC-104 connectors are not completely fixed, and many configuration selections are available to ease integration with existing systems. It is typically used for power supply and a control interface. High-speed data transfers (of image data) are recommended via connector P5. Connectors P2, P3 and P4 provide an internal interface to the FEE.

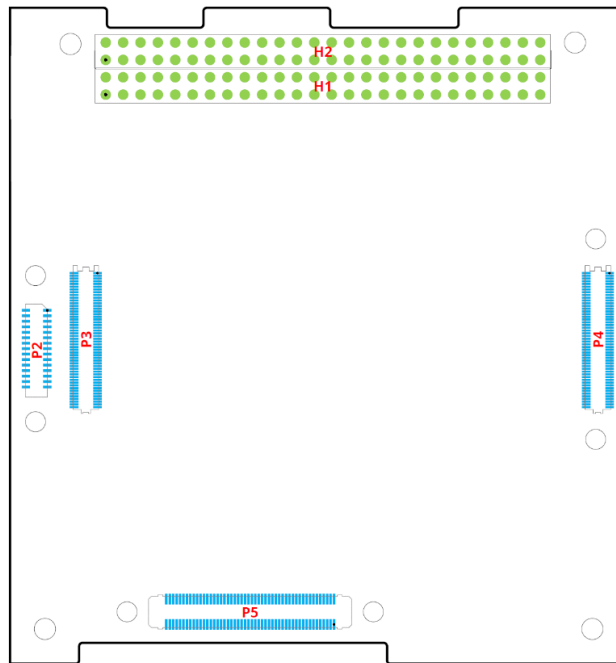


Figure 5-1: CE Connector Locations

5.1 CSKB PC-104 Connector H1 and H2

The standard CubeSat Kit Bus Connectors (H1 and H2) have a pin assignment as shown in Table 5-1 and Table 5-2. It should be noted that due to the diverse configuration selections, several pins appear in the table more than once, according to their configured role.

Table 5-1: Connector H1 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
47, 49, 51	5V_IN	Power	5 V Input Power supply ⁽¹⁾
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16	PowerCtrl	3.3 V Input ⁽²⁾	Power switch user control. High for on, low for off. ⁽³⁾
1	CANL	CAN	Low level CAN bus line ⁽⁵⁾
3	CANH	CAN	High level CAN bus line ⁽⁵⁾
23, 41	SDA	3.3 V I/O ⁽⁴⁾	I ² C serial data

Pin Number(s)	Pin Name	Signal Type	Description
21, 43	SCL	3.3 V Input ⁽⁴⁾	I ² C serial clock
1, 2, 3, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 30, 31, 33, 40	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 29, 32, 35, 39	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 5 pairs)
12, 25, 26, 27, 28, 34, 36, 37, 38, 42, 44, 45, 46, 48, 50, 52	NC	N/A	Not connected.

Table 5-2: Connector H2 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
13, 15, 16, 25, 26	5V_IN	Power	5 V Input Power supply ⁽¹⁾
29, 30, 32	5V_RETURN	Power	5 V Power return
17, 18, 19, 20	PowerCtrl	3.3 V Input ⁽²⁾	Power switch user control. High for on, low for off ⁽³⁾
47	RS422_RX_A	RS-422	RS-422 Receiver A line ⁽⁵⁾
49	RS422_RX_B	RS-422	RS-422 Receiver B line ⁽⁵⁾
48	RS422_TX_A	RS-422	RS-422 Transmitter A line ⁽⁵⁾
50	RS422_TX_B	RS-422	RS-422 Transmitter A line ⁽⁵⁾
21, 22, 47, 48, 49, 50	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
17, 18, 19, 20, 47, 50	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 2 pairs)
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 23, 24, 27, 28, 31, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 51, 52	NC	N/A	Not connected.

- (1) At least one 5 V power supply pin must be used, the rest may remain unconnected (as per the product configuration).
- (2) PowerCtrl input is 5 V tolerant.
- (3) Only one of these pins may be selected (as per the product configuration).
- (4) I²C interface may be configured for 5 V signal levels (as per the product configuration).
- (5) Only available as an option

5.2 High-Speed Connector P5

The primary purpose of the high-density connector P5 is to provide an interface suitable for high-speed data transfers. A total of 9 LVDS pairs are available, but only 5 are used for the High-Speed Data interface, as described in 4.3. These LVDS pairs may also be used to implement a customer-specific interface if required, as a custom option. The connector also provides an alternate power and control (I²C) interface.

Table 5-3: Connector P5 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80, 85	GND	Power	Digital Ground
93, 95, 96, 97, 98, 99, 100	5V_IN	Power	5 V Input Power supply
86, 89, 90, 91, 93, 94	5V_RETURN	Power	5 V Power return
87	PowerCtrl	3.3 V Input ⁽¹⁾	Power switch user control. High for on, low for off.
59	CE_On	3.3 V Output	Power Status. High when CE is on, low when off.
88	SDA	3.3 V I/O ⁽²⁾	I ² C serial data
92	SCL	3.3 V Input ⁽²⁾	I ² C serial clock
58	LVDS0_P	LVDS	High-speed LVDS, Clock+ ⁽³⁾
60	LVDS0_N	LVDS	High-speed LVDS, Clock- ⁽³⁾
64	LVDS1_P	LVDS	High-speed LVDS, Sync+ ⁽³⁾
66	LVDS1_N	LVDS	High-speed LVDS, Sync- ⁽³⁾
69	LVDS2_P	LVDS	High-speed LVDS, D0+ ⁽³⁾
71	LVDS2_N	LVDS	High-speed LVDS, D0- ⁽³⁾
70	LVDS3_P	LVDS	High-speed LVDS, D1+ ⁽³⁾
72	LVDS3_N	LVDS	High-speed LVDS, D1- ⁽³⁾
75	LVDS4_P	LVDS	High-speed LVDS, RR+ ⁽³⁾
77	LVDS4_N	LVDS	High-speed LVDS, RR- ⁽³⁾
76	LVDS5_P	LVDS	High-speed LVDS.
78	LVDS5_N	LVDS	High-speed LVDS.
81	LVDS6_P	LVDS	High-speed LVDS.
83	LVDS6_N	LVDS	High-speed LVDS.
82	LVDS7_P	LVDS	High-speed LVDS.
84	LVDS7_N	LVDS	High-speed LVDS.
63	LVDSaux_P	LVDS	High-speed LVDS.
65	LVDSaux_N	LVDS	High-speed LVDS.
3, 4, 5, 6, 9, 10, 11, 12, 15, 16, 17, 21, 22, 23, 24, 27, 28, 29, 30, 33, 34, 35, 36, 39, 40, 41, 42, 45, 46, 47, 48, 51, 52, 53, 54, 57	Reserved	N/A	Reserved

(1) PowerCtrl input is 5 V tolerant

(2) I²C interface may be configured for 5 V signal levels (as per the product configuration sheet)

(3) LVDS assignments for standard High-Speed Data Interface

6. Electrical Specifications

6.1 Absolute Maximum Ratings

The absolute maximum ratings of the electrical interfaces are shown in Table 6-1. Use of the HyperScape100 beyond the absolute maximum ratings may cause permanent damage.

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
Power Supply				
V _{in}	5 V Input Supply	4.5	5.5	V
GPIOs⁽¹⁾				
V _{GPIO}	Voltage on input/output pin	- 0.5	3.8	V
I²C				
V _{I2C}	Voltage on I ² C pin	- 0.5	7	V
LVDS⁽²⁾				
V _{ICM}	Common-mode input voltage	0.6		V
V _{ID}	Differential input voltage	0.1		V
Power Control				
V _{PC}	High-level input voltage	0	5.0	V

(1) GPIOs include the SPI interface

(2) LVDS signals include the HSIOs and High-Speed Data Interface

6.2 Interface Specifications

The recommended signal levels for the Control Electronics interfaces are given in Table 6-2

Table 6-2: DC Signal Level Specifications

Symbol	Parameter	Min.	Typ.	Max.	Units
Power Supply					
V _{in}	5 V Input Supply	4.75	5.0	5.25	V
GPIOs⁽¹⁾					
V _{IH}	High-level input voltage	2.0	-	3.45	V
V _{IL}	Low-level input voltage	- 0.3	-	0.8	V
V _{OH}	High-level output voltage	2.9	-	-	V
V _{OL}	Low-level output voltage	-	-	0.4	V
I _{SINK} , I _{SOURCE}	Current sink or source per pin	-	-	±10	mA
I²C					
V _{IH(5.0V)}	High-level input voltage @ 5.0 V ⁽³⁾	2.31	-	5.5	V
V _{IH(3.3V)}	High-level input voltage @ 3.3 V ⁽³⁾	2.31	-	3.45	V
V _{IL}	Low-level input voltage	-0.5	-	0.99	V
V _{OL}	Low-level output voltage	-	0.1	0.2	V
LVDS⁽²⁾					
V _{ICM}	Common-mode input voltage	0.6	1.25	2.35	V
V _{ID}	Differential input voltage	0.1	0.35	0.6	V

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{OCM}	Common-mode output voltage	1.125	1.2	1.375	V
V _{OD}	Differential output voltage	0.25	0.35	0.45	V
Power Control					
V _{IH}	High-level input voltage	2.5	3.3	5.0	V
V _{IL}	Low-level input voltage	0.0	-	0.5	V

- (1) GPIOs include the SPI interface
- (2) LVDS signals include the HSIOs and High-Speed Data Interface
- (3) The maximum input voltage depends on the selected I²C voltage (3.3 V or 5.0 V)

The AC characteristics of the interfaces are summarised in Table 6-3.

Table 6-3: AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
SPI					
f _{SPI}	SPI frequency	-	-	10	MHz
I²C					
f _{I2C}	I ² C frequency	-	-	400	kHz
LVDS					
f _{LVDS}	LVDS frequency	-	100	-	MHz
Power Control					
t _{PULSE}	Input pulse width	100	-	-	ms

6.3 Power Consumption

The typical power consumption of the HyperScape100, with a power supply of 5.0 V, is given below, for the beginning of life (BOL) as well as after exposure to radiation (total ionising dose of 25 krad).

Table 6-4: Power Consumption (BOL)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode ⁽¹⁾	470 mA	2.35 W
Imaging Mode ⁽²⁾	1100 mA	5.50 W
Readout Mode ⁽³⁾	470 mA	2.35 W

Table 6-5: Power Consumption (after 25 krad TID)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode ⁽¹⁾	495 mA	2.48 W
Imaging Mode ⁽²⁾	1160 mA	5.80 W
Readout Mode ⁽³⁾	495 mA	2.48 W

- (1) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are static.
- (2) CE and FEE are powered on, and an image is being captured.
- (3) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are active.

7. Environmental Ratings

The HyperScape100 is designed for use in LEO orbit space applications, within the environmental conditions described in Table 7-1.

Table 7-1: Environmental Absolute Maximum Ratings

Description	Value
Operating Temperature	-10 to +50 °C
Survivable Temperature	-25 to +65 °C
Vibration	14.1 g _{rms} (all directions) ⁽¹⁾
Radiation (Total Ionizing Dose)	> 15 krad ⁽²⁾

(1) Based on GSFC-STD-7000

(2) Performance guaranteed to 15 krad. Functional after 15 krad, but performance may be degraded.

8. Physical Characteristics

The physical characteristics of the HyperScape100 are shown in Table 8-1.

Table 8-1: Physical Characteristics

Description	Value
Mass	1.2 kg
Dimensions	98 x 98 x 176 mm

The mechanical drawing in Figure 8-1 below shows the independent mounting points of the OFE hardware and Figure 8-2 shows the standard PC-104 PCB mounting points of the control electronics. . All dimensions are in millimetres (mm).

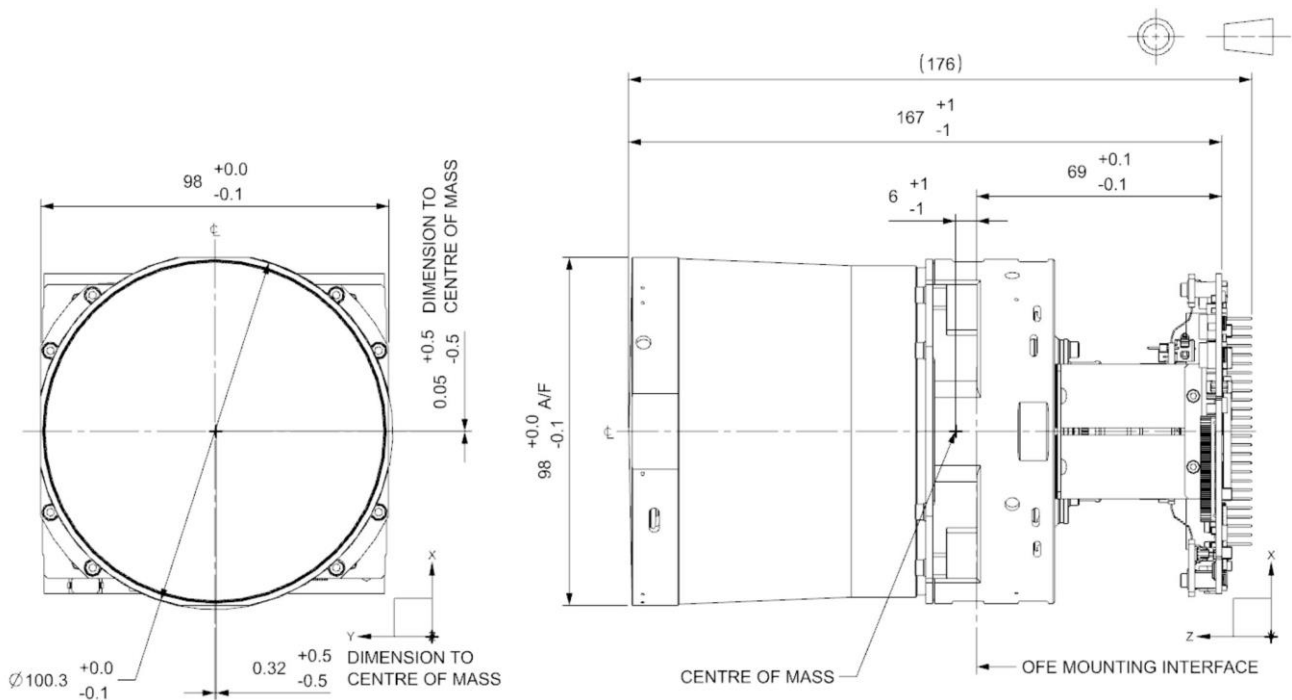


Figure 8-1: Mechanical Drawing

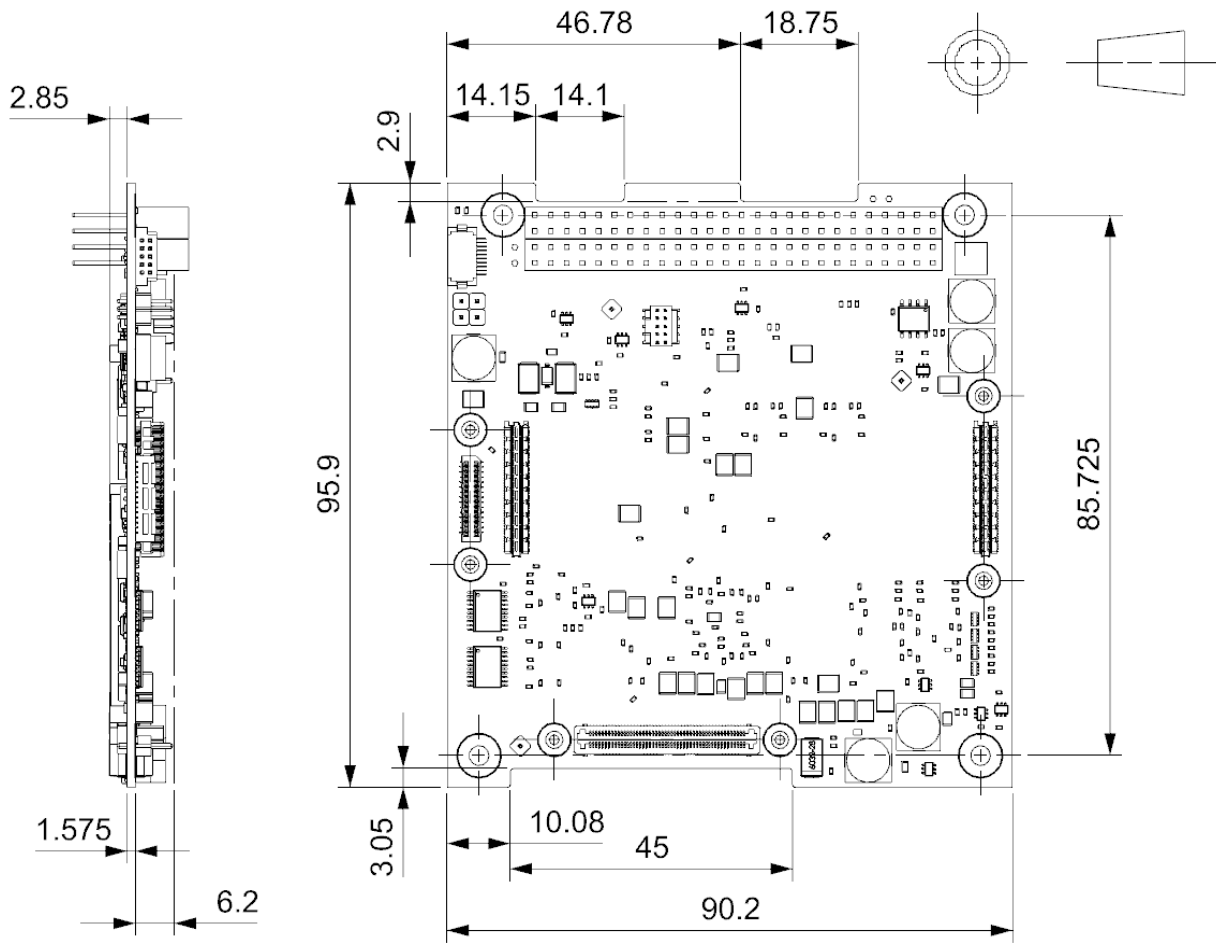


Figure 8-2: CE Mechanical Drawing

Contact Us

Simera Sense (Pty) Ltd

Old Paardevlei Road
Somerset West, 7130
South Africa
sense@simera.com