CNTFET Modeling and Low Power SRAM Cell Design

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***Abstract*— This paper presents compact model for carbon nanotube field effect transistor (CNTFET) which is derived from electronic structure of carbon nanotube (CNT). Complete current transport model is developed from carrier concentration in CNT for different chirality. The model describes the variation of charge developed on CNT with gate voltage. I-V characteristics have been efficiently modeled and compact model is developed for HSPICE circuit simulations. Finally 6T static random access memory (SRAM) cell is designed with developed model and analysis is done for various performance metrics. Results show that CNTFET based 6T-SRAM consumes very less standby power with high static noise margins.**

Keywords- Carbon Nanotube field effect transistor, Modeling, SRAM, HSPICE, Static Noise Margin

I. INTRODUCTION

In recent years, carbon nanotubes (CNTs) have been explored extensively as novel structure material for future semiconductor devices. CNTs act as promising replacement for silicon industry as recent experimental data [1-2] shows considerable improvement over silicon metal oxide semiconductor field effect transistor (MOSFET). Recently it has been demonstrated that CNTFETs are viable option for low power circuit design [3]. Due to extensive electrical properties of CNT that depends on chirality [4], it may act as conductor as well as semiconductor. Due to this, designers are thinking towards completely CNT based circuits [5].

Much work is going on modeling of carbon nanotube field effect transistor (CNTFET) and have been reported in literature [6-10]. For novel molecular electronics devices like CNTFET, it is necessary to develop accurate models, since the standard approximations and models used for MOS electronics may lose their applicability range. Due to different electrical properties of CNT, which includes dependencies of intrinsic carrier concentration and bandgap on diameter of nanotube [11], it is mandatory to precisely understand transport phenomena in CNTFET at the molecular scale. Electron phonon scattering effects play major role in non ballistic transport mechanism [12]. However for smaller channel lengths (~200nm) which are comparable to mean free path of intrinsic CNT [13], ballistic transport may be assumed for modeling.

This paper presents compact model for CNTFET based on electronic structure of CNT. CNT basic properties i.e. bandgap and intrinsic carrier concentration are defined by electronic structure [14]. The approach for modeling the drain current is to make the analytical relation between the charge developed across CNT channel with gate bias. The relation denies the self consistent equations [15] which are responsible for complexity. *I-V* characteristics have been efficiently modeled and simulated using MATLAB. In order to perform the circuit simulations, model file is developed for HSPICE simulator. Lastly 6T static random access memory (SRAM) is designed and simulated in HSPICE. Various performance parameters are evaluated for SRAM namely static noise margin (SNM), read SNM, write SNM and static power dissipation. The paper is organized as follows: Section 2 describes theory for analytical modeling. Section 3 describes the SRAM design and simulations. Lastly conclusions are drawn in Section 4.

II. MODELING THEORY FOR CNTFET

The modeling theory arises from the study of electronic structure. CNTs are the graphene sheets which are rolled around T-axis to form nanotube with diameter in range of *nm*. The way it is rolled decides its electrical property which is defined by chiral vectors (*n,m*). From these chiral vectors, analytical expressions are derived. The diameter can be directly calculated from (*n,m*), which is used to calculate the bandgap and hence value of conduction band minima (Δ_1) [16]. By using these values, intrinsic carrier concentration can be calculated inside CNT channel which is responsible for conduction.

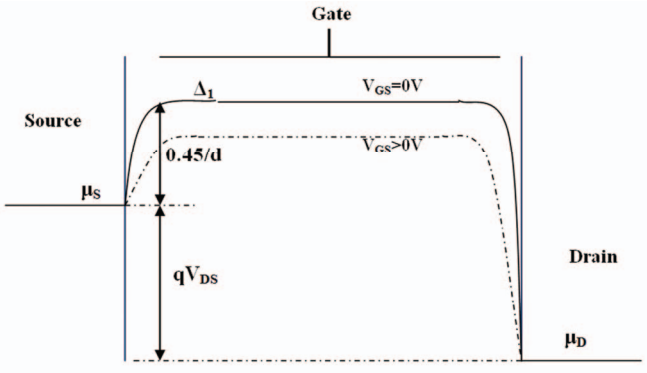

Fig. 1 Band diagram of CNTFET with different V_{GS}

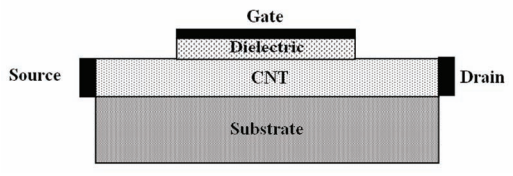

Fig 2. Top gated CNTFET structure

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The model can be explained from Fig.1 in which band of the channel is shifted in downward direction with effect of gate bias. The gate bias induces the charge on the CNT channel which is responsible for potential developed on it. The fermi level of source and drain side will be shifted with effect of drain bias. The drain current (I_{DS}) can be calculated as [17]:

$$I_{DS} = \left(\frac{qKT}{\pi h}\right)[\ln(1+\exp(\xi_S)) - \ln(1+\exp(\xi_D))] \quad (1)$$

where q is electronic charge and h is Planck's constant, K is Boltzman constant, T is operating temperature. The values of ξ_S and ξ_D are given as:

$$\xi_S = \frac{\Delta E_F + q(V_{CNT}(0) - V_{SB} - \varphi_0) - \Delta_1}{KT} \quad (2)$$

$$\xi_D = \frac{\Delta E_F + q(V_{CNT}(L) - V_{DS} - \varphi_0) - \Delta_1}{KT} \quad (3)$$

ΔE_F is the shift in fermi level due to doping, V_{SB} and V_{DS} are the source to body and drain to source bias respectively. V_{CNT} and Φ_0 are the CNT surface potential due to front gate and back gate (body). For top gate device structure (Fig. 2), Φ_0 is set to zero. The value of V_{CNT} is different at source and drain and can be calculated as [18]:

$$V_{CNT}(0) = V_{GS} - V_{FB} \quad (4)$$

$$V_{CNT}(L) = \frac{V_{GS} - \delta I e^{-1} - V_{FB} + \delta m\left(V_{CB} + \varphi_0 + \frac{\Delta_1 - \Delta E_F - KT}{q}\right)}{1+\delta m} \quad (5)$$

where V_{GS} is gate to source bias, V_{CB} is the induced potential between the carbon nanotube and the substrate due to the drain and source terminal voltages and V_{FB} is flat band voltage. The values of m, I and δ can be calculated analytically from [18].

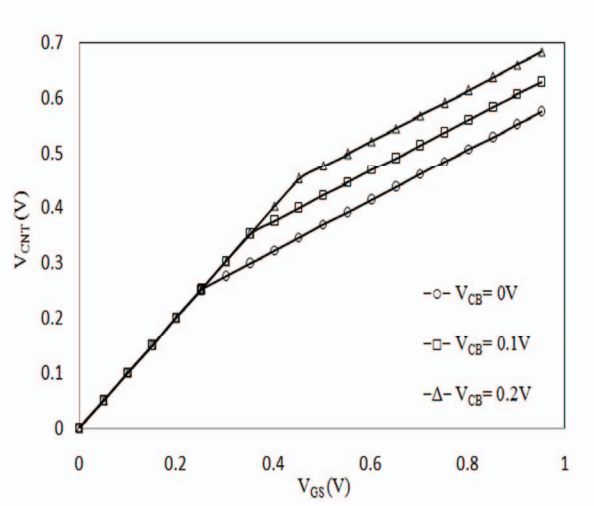

Fig. 3 $V_{CNT} - V_{GS}$ characteristics for different V_{CB}

From the above equations, characteristics have been plotted in MATLAB for (19,0) CNT. The simulations have been performed for top gate structure with oxide thickness of 1nm. V_{CNT} is plotted against V_{GS} for different V_{CB} and V_{FB} (Fig. 3 and 4). It has been clearly demonstrated that V_{CNT} follows V_{GS} *for* V_{GS} less than first conduction band minima (Δ_1). The value of Δ_1 is given by 0.45/d. Hence for (19,0) CNT, d=1.5nm and Δ_1 =0.3V. It can be inferred from the results that V_{CB} and V_{FB} deviates the characteristics from their ideal behaviour. Hence it is preferred to assume their values to be zero for simulations.

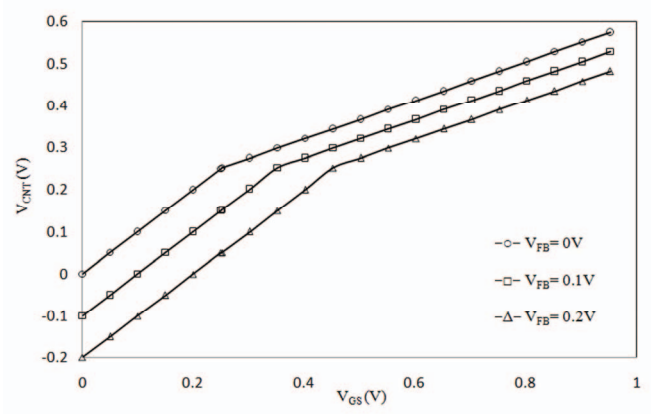

Fig. 4 $V_{CNT} - V_{GS}$ characteristics for different V_{FB}

Fig 5 and 6 shows the $I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$ characteristics for CNTFET. The various parameters taken for simulations are diameter of CNT=1.5nm, oxide thickness=1nm, k=16 for dielectric material. *I-V* characteristics are plotted by taking the values of V_{CB} and V_{FB} as zero for better gate control. Fig. 5 shows better exponential and saturation value for $I_{DS} - V_{DS}$ characteristics. Fig. 6 shows good ON-OFF ratio for $I_{DS} - V_{GS}$ characteristics which proves compatibility for digital circuit applications.

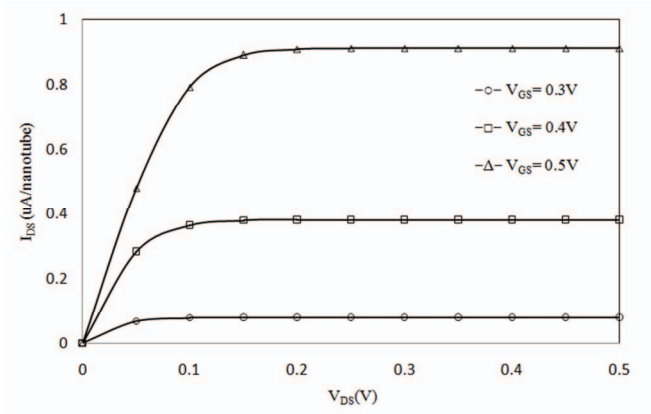

Fig. 5 $I_{DS} - V_{DS}$ characteristics for different V_{GS}

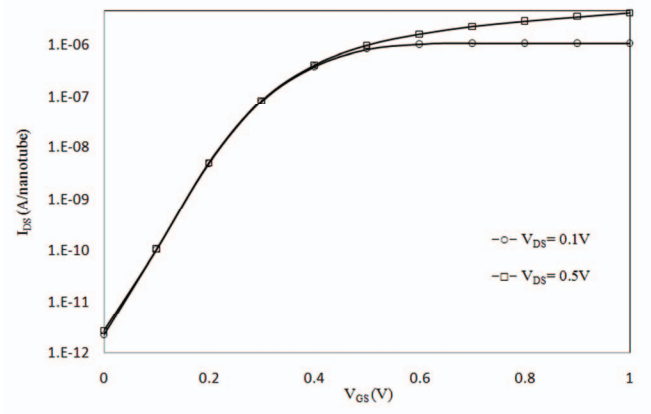

Fig. 6 $I_{DS} - V_{GS}$ characteristics for different V_{DS}

III. 6T SRAM Cell Design

The model described is typically surface charge based model which is used for circuit simulations. To obtain

circuit compatible model, it is important to obtain *I-V* characteristics in terms of V_{GS}, V_{DS} and V_{SB}. Calculation of surface potential on CNT requires self consistent solution which makes circuit simulations impossible. As it is clearly inferred from (4) and (5), proposed model denies self consistent equation and hence it can be used for SPICE simulations. Model has been developed for NCNTFET and PCNTFET and is implemented for SRAM design.

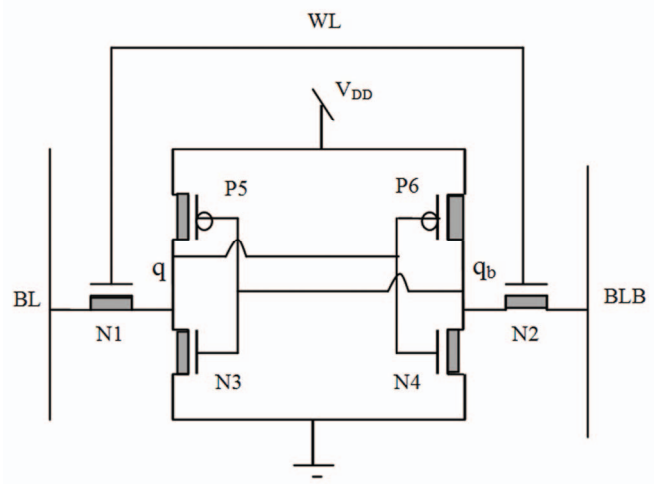

Fig7. 6T CNTFET SRAM cell structure

The 6T CNTFET SRAM cell structure is shown in Fig. 7. It consists of two cross coupled inverters along with two NCNTFET pass transistors. The structure is same as conventional MOSFET structure with MOSFET replaced by CNTFET. Recent research shows that CNTFET based SRAM shows improvement in all performance parameters over conventional CMOS based design [19]. It is due to the reason that SNM depends on threshold voltage of the PFET and NFET. In CNTFET, threshold voltage depends on chrality, which can be used to design novel SRAM cell [20].

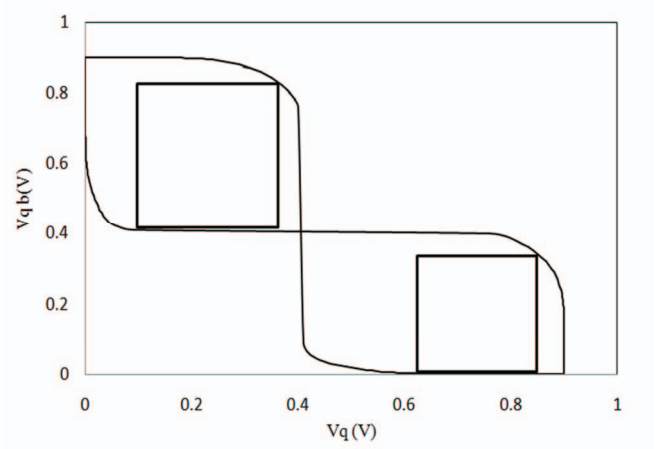

Fig8. SNM for 6T-CNTFET SRAM cell at V_{DD}=0.9V

The performance of the SRAM cell is analyzed by measuring the important figure of merit called SNM. SNM is defined as the maximum voltage amplitude of external signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to diverge from the allowable logic voltage level [21]. The simplest method to measure the SNM is by plotting butterfly curve which results from VTC of the two inverters. The VTC of one inverter is plotted with inverse VTC of second inverter to obtain butterfly curve as shown in Fig 8. SNM can be calculated by measuring the side of longest square that can be fitted between mirrored butterfly curve. The SNM is dependent on the VTC of the cross couple inverters. The standby operation is defined when the cell tends to retain the data value as long as the SRAM cell is supplied by V_{DD}.

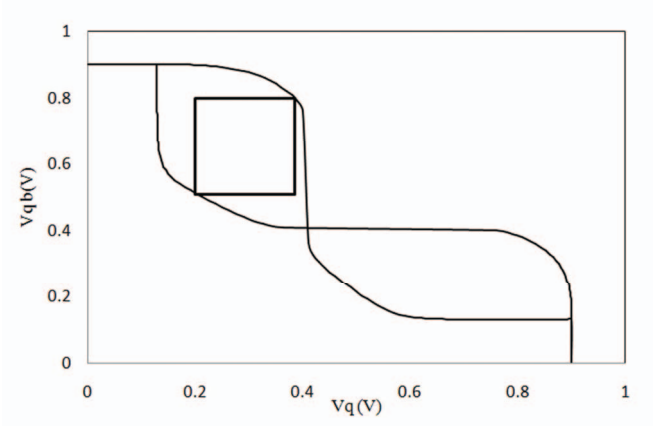

Fig9. Read SNM for 6T-CNTFET SRAM cell at V_{DD}=0.9V

The other figures of merit are read SNM and write SNM which are shown in Fig 8 and 9. Read SNM defines the read ability of SRAM cell i.e. how effectively stored data can be read. Similarly write SNM defines write ability i.e. how easily bit line flip the data stored in SRAM cell. Read SNM and write SNM can be measured similar to SNM using butterfly curve. The only difference is the operation mode i.e. read mode or write mode by activating word line.

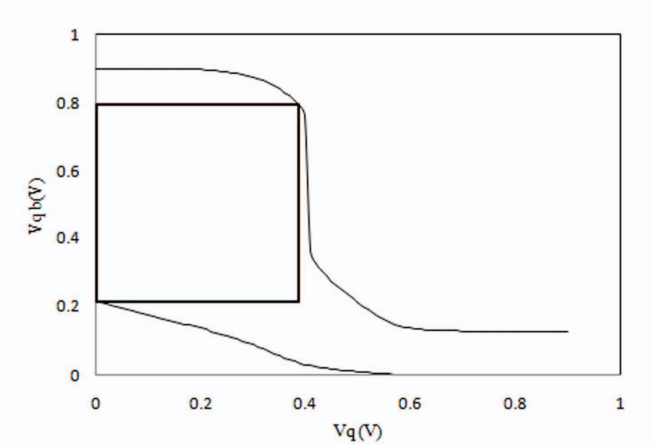

Fig10. Write SNM for 6T-CNTFET SRAM cell at V_{DD}=0.9V

There is need to do proper sizing of PCNTFET and NCNTFET in order to retain voltage at node q and q_b. In CNTFET, sizing can be done by varying number of tubes. For fair results, sizing ratio is taken as P5/N1=P6/N2=0.5 and N4/N2=N3/N1=1.5 from [20]. Table I shows the different performance parameters calculated from simulation for 6TCNTFET SRAM. SNM value finds to be 240mV which is very close to value calculated in [20] hence proved the stability. Read SNM value of 200mV proves stability for reading the data, and highest value of 380 mV of write SNM proves high write stability. Write SNM can be further improved by adjusting the scaling of P5/N1=P6/N2, but it will effect read SNM. Hence there is need to consider tradeoff for better performance. It can be inferred from static power consumption value of 20pW for CNTFET based SRAM cell that CNTFET consumes much less standby power. It is due to reason that very small leakage current (order of pA) flowing through SRAM cell. This proves ultra low power SRAM design is possible with low V_{DD}.

Table I Performance parameters of 6T-CNTFET SRAM cell

Parameters	(19,0) CNTFET SRAM
SNM	240mV
Read SNM	200mV
Write SNM	380mV
Static Power	20pW

IV. CONCLUSION

Compact model for carbon nanotube field effect transistor is presented which is derived from electronic structure of carbon nanotube (CNT). The modelling approach for drain current is based on analytical relation between the charge developed across CNT channel with gate bias. Firstly model is developed for channel potential and effects of flat band voltage and induced potential between the carbon nanotube and the substrate are presented. Through developed model, *I-V* characteristics are plotted for top gate structure in MATLAB. Lastly model is simulated in HSPICE to design 6T SRAM cell and analysis is done for various performance parameters viz. static noise margin (SNM), read SNM, write SNM and static power dissipation. It has been found that CNTFET based SRAM shows superiority in terms of power and stability.

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