Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates

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***Abstract*— In this paper, a new domino circuit is proposed, which has a lower leakage and higher noise immunity without dramatic speed degradation for wide fan-in gates. The technique which is utilized in this paper is based on comparison of mirrored current of the pull-up network with its worst case leakage current. The proposed circuit technique decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits. Thus, the contention current and consequently power consumption and delay are reduced. The leakage current is also decreased by exploiting the footer transistor in diode configuration, which results in increased noise immunity. Simulation results of wide fan-in gates designed using a 16-nm high-performance predictive technology model demonstrate 51% power reduction and at least 2.41× noise-immunity improvement at the same delay compared to the standard domino circuits for 64-bit OR gates.**

***Index Terms*— Domino logic, leakage-tolerant, noise immunity, wide fan-in.**

I. Introduction

DYNAMIC logic such as domino logic is widely used in many applications to achieve high performance, which cannot be achieved with static logic styles [1]. However, the main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the subthreshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates [2] which are typically employed in the read path of register files, L1 caches, match lines of ternary content addressable memories, *Flash* memories, tag comparators, programmable logic arrays, and wide multiplexer-flip-flop (MUX) and De-MUX.

However, in wide fan-in dynamic gates, especially for wide fan-in OR gates, robustness and performance significantly degrade with increasing leakage current. As a result, it is difficult to obtain satisfactory robustness–performance tradeoffs.

Manuscript received October 30, 2011; revised May 2, 2012; accepted May 18, 2012. Date of publication July 19, 2012; date of current version April 22, 2013.

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Digital Object Identifier 10.1109/TVLSI.2012.2202408

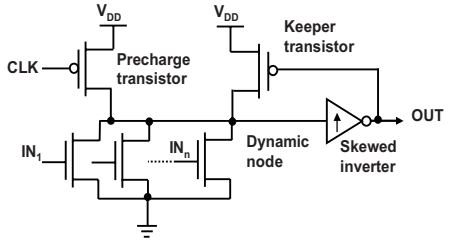

Fig. 1. SFLD adopted from [4].

In this paper, a new current-comparison-based domino (CCD) circuit for wide fan-in applications in ultradeep submicrometer technologies is proposed. The novelty of the proposed circuit is that our work simultaneously increases performance and decreases leakage power consumption.

The rest of this paper is arranged as follows. After the literature review in Section II, the proposed circuit is described in Section III. Section IV includes simulation results for the proposed circuit using HSPICE simulations in the 16-nm V2.1 high-performance predictive technology [3] compared with other conventional circuits. Section V concludes the results.

II. Literature Review

The most popular dynamic logic is the conventional standard domino circuit as shown in Fig. 1. In this design, a pMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node due to the leakage currents and charge sharing of the pull-down network (PDN) during the evaluation phase, hence improving the robustness. The keeper ratio K is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper}-\text{transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{evaluation}-\text{network}}} \tag{1}$$

where W and L denote the transistor size, and μ_n and μ_p are the electron and hole mobilities, respectively. However, the traditional keeper approach is less effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increases current contention between the keeper transistor and the evaluation network.

Thus, it increases power consumption and evaluation delay of standard domino circuits. These problems are more critical

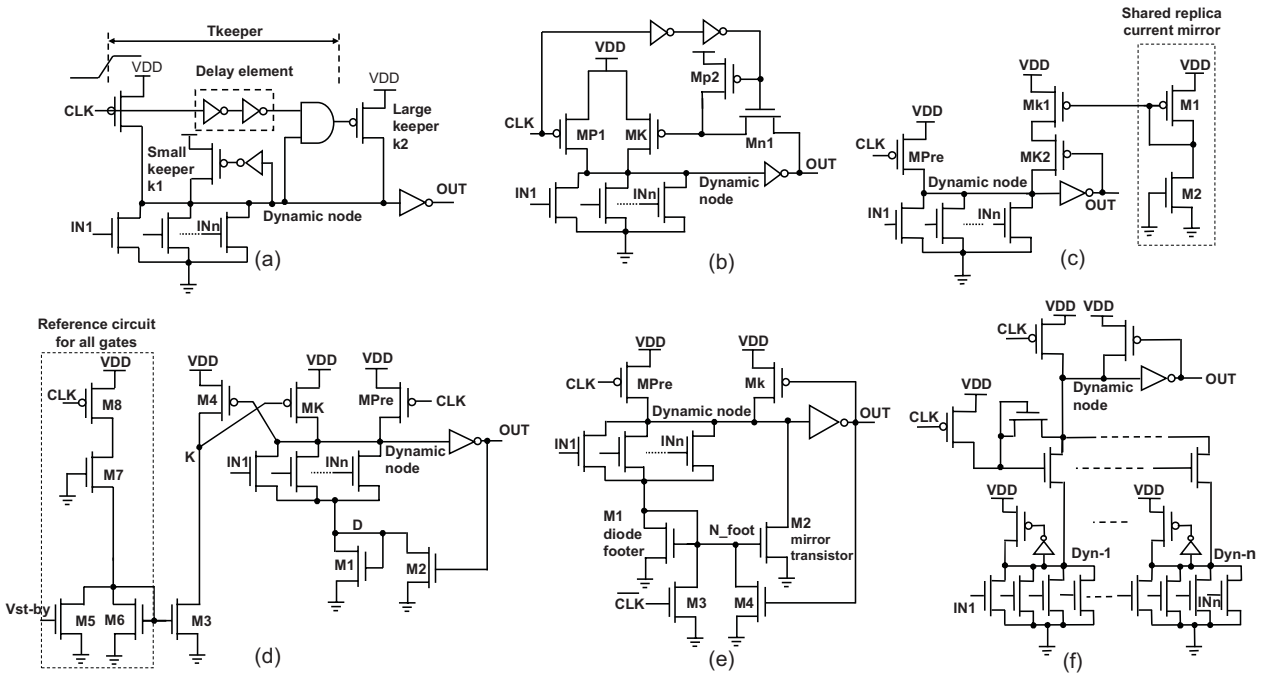

Fig. 2. (a) CKD [5]. (b) HSD [6]. (c) LCR keeper [7]. (d) CKCCD [8]. (e) DFD [4]. (f) DPD [9].

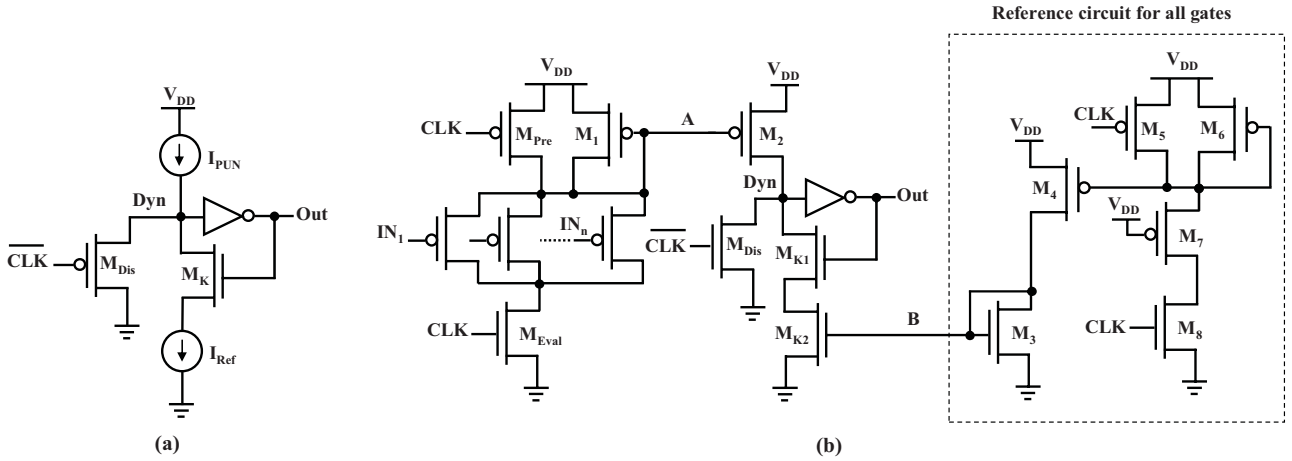

Fig. 3. (a) Concept of proposed circuit (CCD). (b) Implementation of wide OR gate using CCD.

in wide fan-in dynamic gates due to the large number of leaky nMOS transistors connected to the dynamic node. Hence, there is a tradeoff between robustness and performance, and the number of pull-down legs is limited. The existing techniques try to compromise one feature to gain at the expense of the other.

Several circuit techniques are proposed in the literature to address these issues. These circuit techniques can be divided into two categories. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD) [5], high-speed domino (HSD) [6], leakage current replica (LCR) keeper domino [7], and controlled keeper by current-comparison domino (CKCCD) [8], as shown in Fig. 2(a)–(d), respectively. On the other hand, in the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineer the evaluation network such as diode-footed domino (DFD) [4] and diode-partitioned domino (DPD) [9], as shown in Fig. 2(e) and (f), respectively.

III. Proposed CCD Design

Since in wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems would be solved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. This idea is

conceptually illustrated in Fig. 3(a), which utilizes the PUN instead of the PDN. In fact, there is a race between the PUN and the reference current. Transistor M_K is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage.

An important issue in the generation of the reference voltage, which is the correct variation of the reference current according to the process variations to maintain the robustness of the proposed circuit. Process variations are due to random and systematic parameter fluctuations [10]. In random variations, parameters of each device vary individually and independent of adjacent devices. However, systematic variations affect the parameters of neighborhood transistors in the same way, yielding a strong correlation between parameters of nearby devices [11]. In this paper, systematic variations are considered. We have assumed that in a given circuit design the threshold voltage of all nMOS transistors varies together and that of pMOS transistors varies together. In the proposed circuit, effects of any threshold voltage variation on the voltage of nodes A and B [in Fig. 3(b)] is important because it directly affects the speed of the gate, and consequently power consumption and noise immunity. The worst scenario is that the threshold voltage of nMOS transistors is decreased and that of the pMOS transistors is increased, i.e., fast nMOS and slow pMOS due to process variations. In the former case, the subthreshold leakage of pMOS transistors of the PUN is decreased, thus the reference current must be reduced and vice versa for the latter case. Therefore, the reference current must be varied according to threshold voltage variations to maintain robustness in this design. To track process variations in dynamic logic circuits, several solutions are proposed in the literature by using a process variation sensor [12], such as one based on drain-induced barrier lowering (DIBL) effect [11], rate sensing keeper [13], and replica keeper current [7]. In the proposed circuit, a replica circuit like that proposed by [7] can be used as a leakage current sensor for proper operation and superior performance, in the worst case of fan-in, i.e., a 64-input OR gate because of its maximum leakage current among other gates.

The proposed circuit for generation of reference current for all gates is shown in Fig. 3(b). This circuit is similar to a replica leakage circuit proposed by [7], in which a series diode-connection transistor M_6 similar to M_1 is added. In fact, as shown in Fig. 3(b), this circuit was a replica of the worst case leakage current of the PUN to correctly track leakage current variations due to process variations. Therefore, the gate of transistor M_7 is connected to $V_{\rm DD}$, and its size is derived from the sizes of pMOS transistors of the PUN in the worst case, i.e., a 64-input OR gate, and hence its width is set equal to the sum of the widths of 64 pMOS transistors of the PUN.

In the proposed CCD circuit, as shown in Fig. 3(b), current of the PUN is mirrored by transistor M_2 and compared with the reference current, which replicates the leakage current of the PUN. The topology of the keeper transistors and the reference circuit, which is shared for all gates, is similar to that proposed in [7], which successfully tracked the process, voltage and temperature variations. The proposed circuit employs pMOS transistors to implement logical function, as shown in Fig. 3(b). Using the N-well process, source and body terminals of the pMOS transistors can be connected together such that the body effect is eliminated. By this means, the threshold voltage of transistors is only varied due to the process variation and not the body effect. Moreover, utilizing pMOS transistors instead of nMOS ones in the N-well process, it is possible to prevent increasing the threshold voltage due to the body effect in existence of a voltage drop due to the diode configuration of transistor M_1, yielding decreasing the delay.

In other words, one can use nMOS transistors in the P-well process to achieve a higher speed due to their higher mobility. Although slower mobility of pMOS transistors decreases the speed, decreasing the capacitance of the dynamic node in the proposed circuit enables it to increase speed by proper choice of the mirror ratio M [see (2)]. As shown in Fig. 3(b), the proposed circuit has five additional transistors and a shared reference circuit compared to standard footless domino (SFLD). The proposed circuit can be considered as two stages. The first stage preevaluation network includes the PUN and transistors $M_{\rm Pre}$, $M_{\rm Eval}$, and M_1. The PUN, which implements the desired logic function is disconnected from dynamic node Dyn, unlike traditional dynamic logic circuits, and indirectly changes the dynamic voltage. The second stage looks like a footless domino with one input [node A as input in Fig. 3(b)], without any charge sharing, one transistor M_2 regardless of the implemented Boolean function in the PUN, and a controlled keeper consists of two transistors. Only one pull-up transistor is connected to the dynamic node instead of the n-transistor in the n-bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed. The input signal of the second stage is prepared by the first stage. In the evaluation phase, thus, the dynamic power consumption consists of two parts: one part for the first stage and the other for the second stage. As we know the dynamic power consumption directly depends on the capacitance, voltage swing, and contention current on the switching node in the constant condition for frequency, power supply, and temperature. The first stage with n-input has a lower voltage swing $V_{\rm DD}$ to $V_{\rm THP}$ and no contention. On the other hand, the second stage has rail-to-rail voltage swing with minimum contention. Although the proposed circuit has some area overhead, it has less dynamic power consumption compared to footless domino.

Transistor M_1 is configured in diode connection, i.e., its gate and drain terminal are connected together. In the evaluation mode, the current of the PUN transistors establishes some voltage drop across M_1. This voltage will be low, if all inputs are at the high level and only leakage current exists in the PUN and mirror transistor M_2. Otherwise, if at least one conductive path exists between node A and ground, for example, level of one input becomes low in the OR gate, this voltage drop is raised up, turning on mirror transistor M_2 and changing the output voltage.

The voltage drop across transistor M_1 causes the gate-source voltage of the off transistors in the PUN to become positive, yielding an exponential reduction in subthreshold leakage due to the phenomenon called the stacking effect [14]. It should be noted that if the body effect is not eliminated due to the unequal voltage of the source and body terminals, the leakage

current will be decreased further at the expense of higher deviation due to process variations.

The voltage across the diode footer in other domino circuits that use diode-footed techniques such as [4] and [8] must be decreased to zero in order to lower the dynamic node voltage to zero. But in the proposed circuit, it is not necessary for this voltage to reach 0 V since the current of the diode footer is needed instead of the voltage across it. Therefore, the size of the diode-footer transistor M_1 in the proposed circuit is smaller than other DFD circuits. Consequently, a lower leakage current must be compensated by the keeper transistors instead of the larger one in the other circuit due to the larger size of the footer and mirror transistors. This results in lower delay and power consumption and area overhead. On the other hand, in the next predischarge mode, the dynamic node is charged from nonzero voltage to power supply voltage, yielding reduction in the power consumption with respect to existence of the large capacitance on the dynamic node in wide fan-in gates, especially wide fan-in OR gates. In addition, since transistor M_1 increases the switching threshold voltage of the pMOS transistors, the new switching threshold voltage of the gate is about twice the threshold voltage of the pMOS devices [4].

Since upsizing of transistor M_2 increases the speed, the mirror ratio M is defined as the ratio of the size of transistor M_2 to the size of transistor M_1

$$M = \frac{\left(\frac{W}{L}\right)_{M_2}}{\left(\frac{W}{L}\right)_{M_1}}. \tag{2}$$

With reference to the circuit schematic shown in Fig. 3(b), two phases of the proposed circuit are explained in detail as follows.

A. Predischarge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", $\overline{\text{CLK}}$ = "1" in Fig. 3(b)] in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor M_{Dis} and raised to the high level by transistor M_{pre}, respectively.

Hence, transistors M_{pre}, M_{Dis}, M_{k1}, and M_{k2} are on and transistors M_1, M_2, and M_{Eval} are off. Also, the output voltage is raised to the high level by the output inverter.

B. Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", $\overline{\text{CLK}}$ = "0" in Fig. 3(b)] and input signals can be in the low level. Hence, transistors M_{pre} and M_{Dis} are off, transistor M_1, M_2, M_{k2}, and M_{Eval} are on, and transistor M_{k1} can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor M_1 due to the leakage current. Although this leakage current is mirrored by transistor M_2, the keeper transistors of the second stage (M_{k1} and M_{k2}) compensate this mirrored leakage current. It is clear that upsizing the transistor M_1 and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor M_1. This voltage is also equal to drain-source voltage of M_1 and depends on size of M_1 and its current. Increasing the pull-up current increases the mirrored current in transistor M_2, thus voltage of the dynamic node Dyn is charged to V_{DD}, yielding discharging the voltage of the output node and turning off the main keeper transistor M_{k1}. By this technique the contention current between the keeper transistor and the mirror transistor is mitigated. Fig. 4 shows the simulated waveforms of the proposed circuit for the 32-input OR gate. The waveforms are obtained by HSPICE simulator in the 16-nm high-performance V2.1 predictive technology models (PTMs) [3] at 110 °C and 0.8 V supply voltage. In this simulation, only one input of an OR gate with 32 inputs falls to the low level in the evaluation phase. The simulation is performed by setting $W_p/W_n = 2$ for the output inverter, CL = 5 fF, and minimum size for the other transistors.

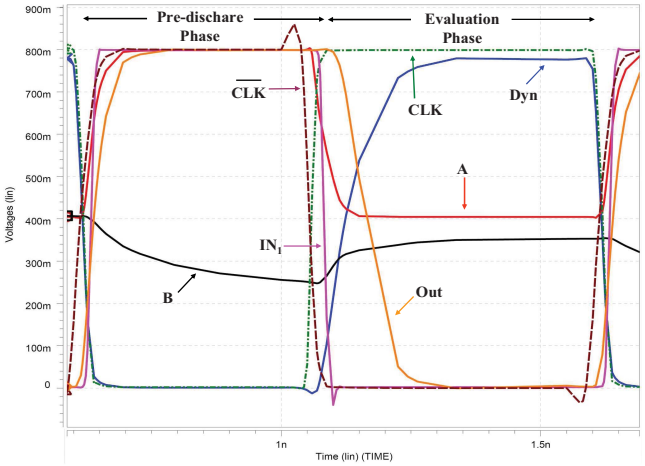

Fig. 4. Simulated waveforms of the 32-input OR gate implemented in the proposed domino circuit.

IV. Simulation Results and Comparisons

The proposed circuit was simulated using HSPICE in the high-performance 16-nm predictive technology [3] and in the bottleneck temperature for technology, i.e., 110 °C. The supply voltage used in the simulations is 0.8 V and the wide fan-in (8, 16, 32, 64 input) OR gate circuit is used as a benchmark, which operates in 1-GHz clock frequency. For the worst case and heavy load due to the high fan-out, the output capacitance load is set at 5 fF.

A. Noise Margin Metric

Several metrics have been proposed in the literature for noise margin of dynamic gates [15]. The noise-margin metric used in this paper is called the unity noise gain (UNG), as used in [2]. It is equal to the amplitude of the input noise that causes the same amplitude to appear at the output. This metric can be shown by

$$\text{UNG} = \{\text{V}_{\text{in}} : \text{V}_{\text{noise}} = \text{V}_{\text{output}}\}. \tag{3}$$

TABLE I
SIZE OF ALL TRANSISTORS OF PROPOSED CIRCUIT FOR 8-, 16-, 32-, AND 64-BIT OR GATE

Fan-in (delay)	W_{k1}	W_{k2}	(W_p/W_n) inverter	W_{Pre}	W_{Eval}	W_{Dis}	W_1	W_2	$(W/L)_3$	W_4	W_5	W_6	W_7	W_8
8-in (50 ps)	7Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	8Lmin	15Lmin/ 2Lmin	7Lmin	7Lmin	7Lmin	64×7Lmin	7Lmin
16-in (50 ps)	8Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	8Lmin	15Lmin/ 2Lmin	7Lmin	7Lmin	7Lmin	64×7Lmin	7Lmin
32-in (60 ps)	8Lmin	9Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	8Lmin	15Lmin/ 2Lmin	7Lmin	7Lmin	7Lmin	64×7Lmin	7Lmin
64-in (70 ps)	7Lmin	7Lmin	14Lmin/ 7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	7Lmin	15Lmin/ 2Lmin	7Lmin	7Lmin	7Lmin	64×7Lmin	7Lmin

TABLE II
COMPARISON OF NORMALIZED UNGS (UNDER SAME DELAY)

Fan-in		Standard footless domino (SFLD)	CKD	High-speed domino (HSD)	Diode-footed domino (DFD)	Leakage current replica (LCR)	Diode-partitioned domino (DPD)	CKCCD	Proposed domino (CCD)
8	UNG (V)	0.41	0.37	0.42	0.67	0.21	0.39	0.63	0.8
	Normalized UNG	1	0.9	1.02	1.63	0.51	0.95	1.54	1.95
16	UNG (V)	0.33	0.31	0.32	0.6	0.27	0.36	0.62	0.8
	Normalized UNG	1	0.94	0.97	1.82	0.82	1.09	1.88	2.42
32	UNG (V)	0.28	0.26	0.27	0.53	0.32	0.35	0.58	0.8
	Normalized UNG	1	0.93	0.96	1.89	1.14	1.25	2.07	2.86
64	UNG (V)	0.22	0.2	0.18	0.49	0.4	0.34	0.53	0.53
	Normalized UNG	1	0.91	0.82	2.23	1.82	1.55	2.41	2.41

In this method, a pulse noise emulates cross-talk type of noise at the input. The level of the input noise can be increased by increasing the noise pulse duration or the noise amplitude. In our simulations, only the input noise amplitude is changed.

B. Definition of Figure of Merit

In order to compare existing circuit techniques with each other, a measure must be used. In the absence of a well-defined and comprehensive figure of merit to account for noise, delay, power, and area together, we have previously proposed a figure of a merit (FOM) for the design of a logic gate such as an OR gate [8]. In this paper, we modified it to consider the process variation as follows:

$$\text{FOM} = \frac{\text{UNG}_{\text{norm}}}{P_{\text{tot}-\text{norm}} \times t^2_{P-\text{norm}} \times \sigma_{\text{Delay}-\text{norm}} \times A_{\text{norm}}} \quad (4)$$

where UNG_{norm}, $t_{\text{P}-\text{norm}}$, $\sigma_{\text{Delay}-\text{norm}}$, and A_{norm} are the UNG, worst case propagation delay, standard deviation of delay, and total area of circuit, respectively, each of which is normalized to the value for the 64-input SFLD OR gate. $P_{\text{tot}-\text{norm}}$ represents the normalized average total power including the switching, short-circuit, and leakage power. One of the most critical parameters is EDP or average of the energy-delay product, which is equal to $P_{\text{avg}} \times t_P^2$ according to [1, eq. (5–65)]. Therefore, we have squared the time delay to consider this parameter. As mentioned in [8], use of powers other than those used here for the five factors of interest is also possible.

C. Transistor Sizing

The SFLD (Fig. 1), CKD [Fig. 2(a)], HSD logic circuit [Fig. 2(b)], LCR keeper [Fig. 2(c)], CKCCD [Fig. 2(d)], DFD [Fig. 2(e)], and DPD [Fig. 2(f)] are simulated to compare with the proposed CCD circuit [Fig. 3(b)]. Since wide fan-in (8, 16, 32, 64 input) OR gates are implemented by using these circuits in the same delay, i.e., 50, 50, 60, and 70 ps delay for 8, 16, 32, and 64 in the OR gate, respectively. Thus, sizing of the transistors is done to achieve these desired delays. For all circuits, the width of the transistors in the OR gate block is set to the minimum width, which is equal to $W_{\text{min}} = 7L$ min, where $L_{\text{min}} = 16$ nm. The width ratio of pMOS to nMOS transistor of the inverters is set to 2, except those are specified below. The length of all transistors and the width of other transistors are set to minimum size and are necessarily varied to achieve the desired delay.

In the SFLD (Fig. 1), the keeper size is increased from 0.1 to 1 times the evaluation transistor size [(i.e., increasing keeper ratio k in (1)] to extract different data points for delay, and UNG. The precharge transistor in Fig. 1 is upsized, if it is necessary to achieve the desired delay. For the CKD [Fig. 2(a)], the length of the transistors of the inverters, which is utilized as a delay element, is set to $2L$min to provide useful delay T_{keeper}. The tradeoff between performance and UNG in the conditional-keeper circuits is achieved by varying the delay of T_{keeper} in Fig. 2(a), which is done by upsizing its inverters.

The width ratio of pMOS to nMOS transistor of the output inverter is set to 1 and the width of small and large keeper

TABLE III
COMPARISON OF POWER CONSUMPTION NORMALIZED TO SFLD UNDER SAME DELAY

Fan-in		Standard footless domino (SFLD)	Conditional-keeper domino (CKD)	High-speed domino (HSD)	Diode-footed domino (DFD)	Leakage current replica (LCR)	Diode-partitioned domino (DPD)	CKCCD	Proposed domino (CCD)
8	Power	12.6	12.9	19.1	12	12.7	10.8	9.2	8.3
	Normalized power	1	1.02	1.52	0.95	1.01	0.86	0.73	0.66
16	Power	12.9	13.6	17.6	12.7	13	14	9.2	8.6
	Normalized power	1	1.05	1.36	0.98	1.01	1.09	0.71	0.67
32	Power	15.7	17	20.5	14.8	16	21.6	10.7	9.1
	Normalized power	1	1.08	1.31	0.94	1.02	1.38	0.68	0.58
64	Power	19.4	20.3	19.4	19	19.3	33	13.4	9.5
	Normalized power	1	1.05	1	0.98	0.99	1.7	0.69	0.49

transistors are varied to obtain the desired delay. The width of pMOS transistors in the static NAND gate is two times nMOS counterparts.

The inverters of the gates, which are simulated using the HSD, have minimum length and the width ratio of pMOS to nMOS transistor of output inverter is set to 1. To obtain the desired delay, the widths of keeper transistor M_K and transistors M_{n1} and M_{p1} are varied.

The length of transistor M_1 in the shared replica current mirror in Fig. 2(c) is set to $7L\text{min}$ to eliminate channel length modulation and reduce variation of the threshold voltage. The width of transistor M_2 is equal to the sum of the widths of the nMOS transistors of the PDN. The width of the keeper transistors of the gates, which are simulated using the LCR keeper are varied to obtain the given delay.

In the CKCCD circuit [Fig. 2(d)], the width of transistors M_6, M_7, and M_8 are chosen such that the leakage current of the reference circuit is slightly higher than that of a 64-input OR gate. The width of mirror transistor M_3 should be equal to or less than the width of M_6 to reduce the contention between M_4 and M_3. To achieve maximum speed $W_{1\,\text{min}} = 10\ W_{\text{pull-down}}$, where $W_{\text{pull-down}}$ is the width of the transistors in the wide OR gate block.

For the DFD [Fig. 2(e)] gates, the desired delay is achieved by varying the size of the mirror, keeper, and precharge transistors.

In the DPD [Fig. 2(f)], according to [9] each partition consists of four legs to obtain the best results. All inverters and keepers of the partitions are set to minimum size and the length of the main keeper transistor M_K. The desired delay is achieved by varying the size of the precharge and keeper transistors.

The W/L of transistor M_3 in the proposed CCD circuit [Fig. 3(b)] is set to 15/2 to mitigate channel length modulation and V_{th} variation, like the LCR keeper, and width of other transistors of the reference circuit is chosen to produce leakage current corresponding to a 64-bit OR gate. In the absence of the industrial technology model for the 16-nm process, the area of the additional circuit is estimated to be 0.506 fm^2. As shown in Table I, by varying the width of the mirrorand keeper transistors, the desired delays t_d, i.e., 50, 50, 60, and 70 ps can be achieved for 8, 16, 32, and 64 in the OR gate, respectively.

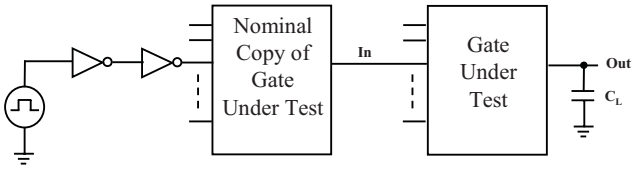

Fig. 5. Simulation framework used in this paper [16].

D. Simulation Framework

The wide fan-in (8, 16, 32, 64 input) OR gate circuit into a framework [16] is used as a benchmark, as shown in Fig. 5. As shown in the figure, the logic gate under test is driven with a nominal copy of it to provide a realistic input waveform. For performance measurement, the delay from input IN to output OUT of the gate under test is measured in the evaluation phase while one input changes and all other inputs remain at the previous state. The same is performed for measuring power consumption and UNG of the gate under test. Also to evaluate the impact of process variations, Monte Carlo simulations are done on all transistors in this framework.

Numerical results for UNGs are shown in Table II. All simulations are performed in the same delay for a specific fan-in. The results obtained indicate from 1.95 to 2.41 times improvement over the SFLD, indicating that the proposed circuit has a better noise immunity compared with the rest.

Table III shows a comparison of power consumption (which is normalized to power consumption of the SFD domino OR gate) with other techniques. It shows a reduction in normalized power consumption from 33% to 51% compared to the SFLD. To consider process variations, variations of delay, and power of a 64-in OR gate, which is implemented in the proposed circuit and the other circuits simulated via Monte Carlo are shown in Tables IV and V, respectively. It must be noticed that gate capacitance fluctuations due to the channel length variation are ignored in this paper and threshold fluctuations are considered the only significant source of variations, as explained in [11]. Other effects such as DIBL and gate tunneling leakage are also tracked by the reference circuit because, as shown in Fig. 3(b), the drain-source voltage of M_7 is equal to that of pMOS transistors of the PUN and consequently, they have the same V_{DS}. On the other hand, the

TABLE IV
EFFECT OF THRESHOLD FLUCTUATIONS DUE TO PROCESS VARIATION ON DELAY FOR 64-BIT OR GATE

Variation (σ_{Vth}/μ_{Vth})	Variable	Standard footless domino (SFLD)	Conditional-keeper domino (CKD)	High-speed domino (HSD)	Diode-footed domino (DFD)	Leakage current replica (LCR)	Diode-partitioned domino (DPD)	CKCCD	Proposed domino (CCD)
1%	μ_{Delay} (ps)	74.4	71.1	68.87	73.1	70.2	73	70.84	72.3
	σ_{Delay} (ps)	1.16	2.6	1.47	3.4	1.45	2.16	1.5	1.7
3%	μ_{Delay} (ps)	74	73.3	70.06	74.1	70.3	73.8	71.2	74.1
	σ_{Delay} (ps)	4	7.64	3.13	8.4	3.54	6.95	4.6	5.5
5%	μ_{Delay} (ps)	73.8	76.8	70.6	76	70.9	77.6	71.6	75.9
	σ_{Delay} (ps)	6.04	24.8	5.4	15	5.47	15.7	8	9.7
7%	μ_{Delay} (ps)	74.2	78.1	71.3	80.23	71.16	82.52	72.46	78.4
	σ_{Delay} (ps)	8.6	22.42	7.7	26	7.5	25.6	11.1	14

TABLE V
EFFECT OF THRESHOLD FLUCTUATIONS DUE TO PROCESS VARIATION ON POWER FOR 64-BIT OR GATE

Variation (σ_{Vth}/μ_{Vth})	Variable	Standard Footless Domino (SFLD)	Conditional-Keeper Domino (CKD)	High-Speed Domino (HSD)	Diode-Footed Domino (DFD)	Leakage Current Replica (LCR)	Diode-Partitioned Domino (DPD)	CKCCD	Proposed Domino (CCD)
1%	μ_{Power} (μw)	19.87	20.5	19.46	19.35	19.75	33.2	13.35	9.5
	σ_{Power} (μw)	0.51	1.5	0.39	0.39	0.48	1.7	0.23	0.28
3%	μ_{Power} (μw)	20.02	28.5	19.53	19.36	19.58	33.55	13.56	9.55
	σ_{Power} (μw)	1.21	21.3	1.14	1.1	1.4	5.2	0.67	0.84
5%	μ_{Power} (μw)	20.2	34.96	19.58	19.67	19.67	34.53	13.67	9.6
	σ_{Power} (μw)	2.1	29.15	1.94	1.91	2.36	8.83	1.1	1.4
7%	μ_{Power} (μw)	20.43	37.05	19.82	20.17	19.88	36.16	13.76	9.75
	σ_{Power} (μw)	2.94	31.6	2.7	2.87	3.43	12.95	1.62	2
10%	μ_{Power} (μw)	21	39.7	20.3	20.59	20.3	39.72	14.1	10
	σ_{Power} (μw)	4.4	35.3	4.1	5.4	5.1	20.3	2.49	3.1

TABLE VI
COMPARISON OF NORMALIZED FOM IN 64 INPUTS OR GATE UNDER SAME DELAY

	Standard Footless Domino (SFLD)	Conditional-Keeper Domino (CKD)	High-Speed Domino (HSD)	Diode-Footed Domino (DFD)	Leakage Current Replica (LCR)	Diode-Partitioned Domino (DPD)	CKCCD	Proposed Domino (CCD)
# of Transistors	68	79	76	72	69	134	74	73
Standard Deviation of Delay	12	19.7	11.04	35	10.6	33.48	17.85	20.4
Normalized Standard Deviation of Delay (ps)	1	1.64	0.92	2.92	0.88	2.79	1.49	1.7
Area (fm^2)	127	169	137	171	144	223	198	133
Normalized Area	1	1.33	1.08	1.35	1.14	1.76	1.56	1.05
Power (μw)	19.4	20.3	19.4	19	19.3	33	13.4	9.5
Normalized Power	1	1.05	1	0.98	0.99	1.7	0.69	0.49
Normalized Delay	1	1	1	1	1	1	1	1
UNG (V)	0.22	0.2	0.18	0.49	0.4	0.34	0.53	0.53
Normalized UNG	1	0.91	0.82	2.23	1.82	1.55	2.41	2.41
FOM	1	0.4	0.83	0.58	1.83	0.19	1.5	2.76

gate leakage of M_3 is negligible compared to the mirrored subthreshold current of M_7 due to the small size of M_3, especially if a small number of gates are connected to the same reference circuit. In these tables, μ and σ are the mean value and standard deviation of the given variable, respectively, and Monte Carlo simulations are performed using

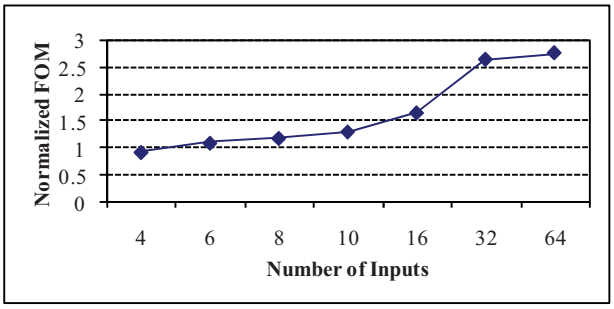

Fig. 6. Relationship between normalized FOM of proposed circuit and number of inputs.

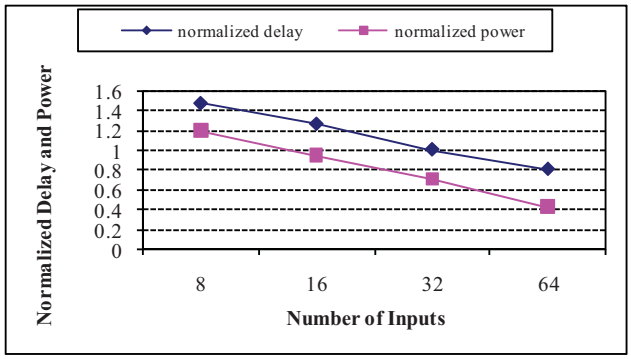

Fig. 7. Relationship between normalized delay and power consumption of proposed circuit in terms of number of inputs under same UNG.

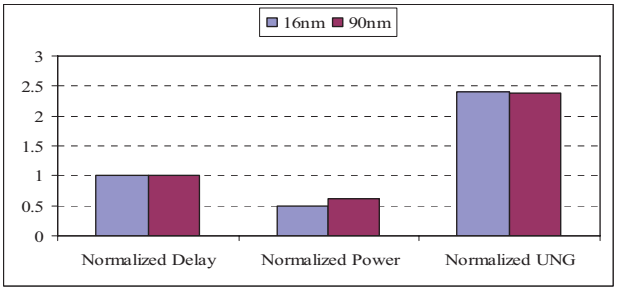

Fig. 8. Relationship between normalized delay, power consumption, and UNG of proposed circuit in two technology nodes.

a Gaussian distribution of the threshold voltage of devices with $3\sigma_{Vth0}$ deviation on the initial threshold voltage V_{th0}. The Monte Carlo simulations are performed in the same manner as done in [11]. The standard deviation of the threshold or the 1-sigma of V_{th} is varied from 1% to 10% of the initial value of V_{th} for all simulations. Although the proposed circuit has relatively high deviation, as shown in Table IV, it has low power, low area, and high noise immunity. Also, according to Table V, the proposed circuit has the lowest deviation on the power consumption, which makes it useful for low-power applications such as sensor networks and portable devices.

In Table VI, the FOM of the simulated circuits are summarized to determine, which circuit technique is better. All the examined circuits were simulated in the 64-input OR gate under the same delay of 70 ps and with 10% standard deviation of the threshold voltage for Monte Carlo simulations.

To consider the improvements, all data are normalized to the FOM of the SFLD counterparts. One can compare several structures with several scenarios, such as performing the simulations for the same UNG, delay, power, or yield. There are mainly two definitions for yield in literature, die yield [1] and time yielding [17]. Die yield is defined as the number of good dies on a wafer and the percentage of those that are functional and generally depends on the die area and the process variations. Time yielding is defined as percentage of the total number of circuits, which meet the desired target delay constraint in spite of process variations. Therefore, both die area and process variations are important to obtain a suitable yield. As a result, when an FOM is defined that takes into account the critical parameters, i.e., UNG, delay, power, and process variations together, the scenario type is not crucial because of the existing strong correlations between those parameters. Therefore, we simulated circuits with the same delay for comparisons because of simplicity.

Moreover, the standard deviation of the threshold voltage was used to consider die-to-die variations for MOS devices in a given circuit. As seen in Table VI, the proposed circuit has the best FOM, because it provides the best UNG, and the least power and area overhead due to the small size of most transistors in spite of further deviation compared to some designs such as LCR keeper. To take the layout penalty of the PUN, which is implemented in the N-well process, into account, one can increase the given area. For example, if the area of the proposed circuit is increased by 50% in the worst case, the FOM of the proposed circuit will be decreased by 33% and will reach to 1.87, which is still greater than others.

In Fig. 6, the proposed FOM is illustrated as a function of the number of inputs to determine the minimum number of inputs, above which the proposed scheme adds a benefit. In fact, due to the area overhead of the proposed circuit, the minimum number of inputs is limited to 6. Furthermore, if the estimated area is increased by nearly 30% due to the use of N-well to implement the PUN, the minimum number of inputs is increased to 10. The relationship between the number of inputs and the reduction in the time delay and power consumption of the proposed circuit, which are normalized to SFLD counterparts, are illustrated in Fig. 7 in the same UNG of 0.24 V or $30\%V_{DD}$. As shown in this illustration, the proposed circuit has lower power consumption and delay if the number of inputs is greater than 16 and 32. This is because the SFLD circuit generally has lower UNG than the proposed circuit. Therefore, if high UNG is needed, the SFLD circuit will not be useful.

The effect of CMOS technology scaling on the proposed circuit and SFLD circuit is examined using a real technology model for the 90-nm node in typical process at the 1.2 V power supply. The power consumption and UNG of the proposed circuit are normalized to SFLD counterparts in the same delay and plotted in Fig. 8. As shown in this figure, the normalized power is still lower and the normalized UNG is greater than those of SFLD.

To consider process, voltage, and temperature variation effects on the proposed circuit CCD, the proposed circuit is simulated using a real 90-nm technology model in four

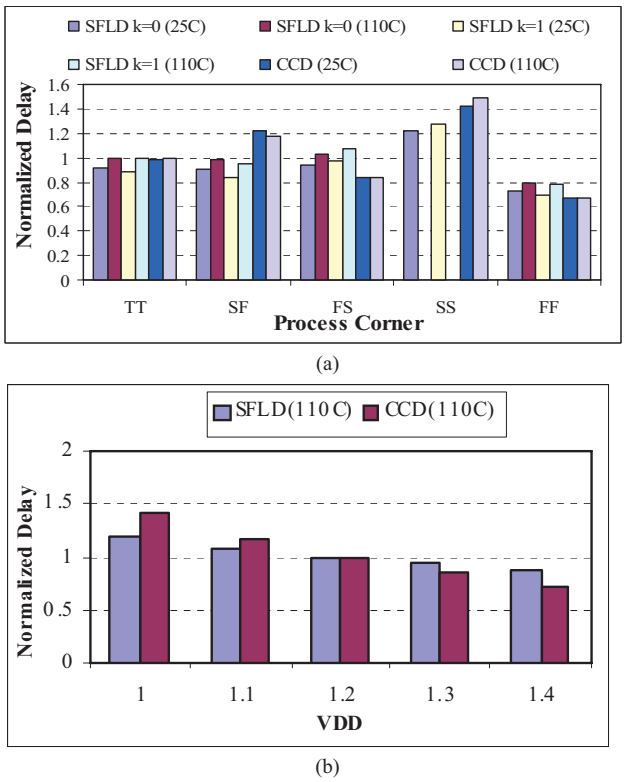

Fig. 9. Variation effects on the normalized delay of proposed circuit (CCD). (a) Process and temperature variation effects. (b) V_{DD} variation effect.

process corners and two temperatures at V_{DD} from 1 to 1.4 V. Simulation results for the normalized delay are illustrated in Fig. 9(a) and (b) for two different temperatures in all process corners at 1.2 V and for variable V_{DD} varied from 1 to 1.4 V at 110 °C in typical process. In Fig. 9(a), the time delay of CCD, SFLD with no keeper and with the worst case sized keeper is normalized to the delay of those circuits at 1.2 V in typical process at 110 °C. In Fig. 9(b), the time delay is normalized to the delay of the proposed circuit at 1.2 V in typical process at 110 °C. As shown in Fig. 9(b), the proposed circuit is sensitive to V_{DD} variations. Simulation results show that the standard deviations of 0.1 and 0.16 in V_{DD} result in the standard deviations of 0.16 and 0.27 in the normalized delay of the proposed circuit, respectively. However, as shown in these figures, the proposed circuit works with process, voltage, and temperature variations. The proposed circuit demonstrates superior performance in high-performance PTMs and in the real technology model of 90 nm, but if V_{TH} is about reached to $V_{DD}/2$, the proposed circuit has a lower performance due to the voltage drop across the diode-connection transistor. This voltage drop is used to decrease the overall leakage and enhance the noise immunity in ultradeep-submicrometer technology with lower threshold voltage. To solve this problem, several solutions exist, for example, increasing the source voltage of M_2 by utilizing dual supply voltage, increasing the width of M_2, and increasing the length of M_1 or a composition of these solutions.

The proposed circuit has a low leakage current when all inputs are at the high level and meets the high robustness requirements of wide gates. This is because of the existence of a voltage drop in the sources of the PUN transistors, due to the diode configuration of transistor M_1 whose gate-source voltage is equal to its drain-source voltage. The source voltage of the PUN transistors plays a critical role in lowering the overall leakage in the proposed circuit.

The major factor of the leakage is the subthreshold current, which is given by

$$I_{\text{sub\_th}} = I_0 \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) e^{\left(\frac{V_{GS}-V_{TH}+\eta V_{DS}}{nV_t}\right)} \tag{5}$$

with

$$I_0 = \mu_0 C_{OX} \frac{W}{L}(n-1)V_t^2 \tag{6}$$

where V_{GS} is the transistor gate-source voltage, V_{DS} is the transistor drain-source voltage, V_{TH} is the threshold voltage, $V_t = kT/q$ is the thermal voltage, η is the DIBL coefficient, n is the subthreshold swing coefficient of the transistor, μ_0 is the zero bias mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the transistor. In normal footed domino circuits, when all inputs are at the low level in the evaluation phase, V_{GS} is equal to zero. But in the proposed circuit, when all inputs are at the high level in the evaluation phase and voltage of node A [in Fig. 3(b)] is decreased due to the leakage current, V_{SG} of the PUN transistors will be negative, yielding lower subthreshold leakage current according to the above equations. As a result, decreasing the voltage of node A due to the leakage current prohibits further voltage drop. Simulation results for leakage power indicate that the proposed circuit has a lower leakage current by a factor of 0.43 when all evaluation network transistors are off and clock is at the high level and at 110 °C.

V. Conclusion

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially in wide domino gates, yielding reduced noise immunity and increased power consumption. Thus, new designs were necessary to obtain desired noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only reduced the worst case delay, it also increased the contention between the keeper transistor and the evaluation network. A new circuit design that we called CCD was proposed in this paper. The main goal was to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption. This was done by comparing the evaluation current of the gate with the leakage current. By using this technique, the proposed domino circuit reduced the parasitic capacitance on the dynamic node and keeper size of very high fan-in gates. Using the high-performance PTM V2.1 of 16 nm [3] at a power supply of 0.8 V, wide fan-in 8- to 64-bit OR gate circuits were used as a benchmark. The proposed design plus several existing circuit designs were simulated and compared. Simulation results demonstrated significant progress in leakage reduction and acceptable speed for high-speed applications. Furthermore, they demonstrated that the proposed circuit had a very high UNG for wide fan-in OR gates compared to

other designs. Thus, the proposed CCD was especially suitable for implementing wide fan-in Boolean logic functions with high noise immunity, lower area consumption, time delay, and power consumption.

Moreover, a normalized FOM, previously proposed by the authors, was modified to include standard deviation of delay. The proposed circuit demonstrated FOM of 2.76 times its counterparts in footless domino OR gates for the 64-bit OR gate. Therefore, the proposed circuit was superior to existing designs that were studied in detail in this paper, especially for wide fan-in gates.

REFERENCES

[1] J. M. Rabaey, A. Chandrakasan, and B. Nicolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.

[2] L. Wang, R. Krishnamurthy, K. Soumyanath, and N. Shanbhag, "An energy-efficient leakage-tolerant dynamic circuit technique," in *Proc. Int. ASIC/SoC Conf.*, 2000, pp. 221–225.

[3] *Predictive Technology Model (PTM). 16 nm High Performance V2.1 Technology of PTM Model*. (2012, Feb. 19) [Online]. Available: http://www.eas.asu.edu/~ptm/

[4] H. Mahmoodi and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 3, pp. 495–503, Mar. 2004.

[5] A. Alvandpour, R. Krishnamurthy, K. Sourrty, and S. Y. Borkar, "A sub-130-nm conditional-keeper technique," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 633–638, May 2002.

[6] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 10, no. 2, pp. 71–78, Apr. 2002.

[7] Y. Lih, N. Tzartzanis, and W. W. Walker, "A leakage current replica keeper for dynamic circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 48–55, Jan. 2007.

[8] A. Peiravi and M. Asyaei, "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, integration," *VLSI J.*, vol. 45, no. 1, pp. 22–32, 2012.

[9] H. Suzuki, C. H. Kim, and K. Roy, "Fast tag comparator using diode partitioned domino for 64-bit microprocessors," *IEEE Trans. Circuits Syst.*, vol. 54, no. 2, pp. 322–328, Feb. 2007.

[10] K. Bowman, S. G. Duval, and J. D. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 183–190, Feb. 2002.

[11] H. F. Dadgour and K. Banerjee, "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic or gates," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 18, no. 11, pp. 1567–1577, Nov. 2010.

[12] C. H. Kim, K. Roy, S. Hsu, R. Krishnamurthy, and S. Borkar, "A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 14, no. 6, pp. 646–649, Jun. 2006.

[13] R. G. David Jeyasingh, N. Bhat, and B. Amrutur, "Adaptive keeper design for dynamic logic circuits using rate sensing technique," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 19, no. 2, pp. 295–304, Feb. 2011.

[14] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[15] N. Shanbhag, K. Soumyanath, and S. Martin, "Reliable low-power design in the presence of deep submicron noise," in *Proc. ISLPED*, 2000, pp. 295–302.

[16] M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect of process variations on the delay of static and domino logic," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 18, no. 5, pp. 697–710, May 2010.

[17] H. Mostafa, M. Anis, and M. Elmasry, "Novel timing yield improvement circuits for high-performance low-power wide fan-in dynamic OR gates," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 1785–1797, Aug. 2011.

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