Enhanced Ground Bounce Noise Reduction In a Low Leakage 90nm 1-Volt CMOS Full Adder Cell

Manisha Pattanaik
Department of I.T.
ABV-IIITM
Gwalior,India
e mail:manishapattanaik@iiitm.ac.in

Shantanu Agnihotri
Department of I.T.
ABV-IIITM
Gwalior,India
e mail:shantanugifted786@yahoo.co.in

M.V.D.L.Varaprashad
Department of I.T.
ABV-IIITM
Gwalior,India

T.Anand Arasu
Department of ECE
MANIT
Bhopal,India

Abstract— **In nanometer regime, ground bounce noise and noise immunity are becoming important metric of comparable importance to the leakage current and active power for the analysis and design of complex arithmetic logic circuits. In this paper, low leakage 1bit full adder cell is proposed for mobile applications with low ground bounce noise. A novel approach has been introduced with stacking power gating technique for further reduction in the peak of ground bounce noise during the sleep to active mode transition. The simulation results depicts that the proposed design leads to efficient 1bit full adder cell in terms of standby leakage power, active power, ground bounce noise and propagation delay. We have performed simulations using Cadence Spectre 90nm standard CMOS technology at room temperature with supply voltage of 1V.**

Keywords—**Leakage power; Stacking power gating; Ground bounce noise; sleep transistor and Adder cell.**

I. INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition [1], [2].The adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology [3], [4]. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not only related to ensuring correct circuit operation, but also related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When an electronic device such as a mobile phone is in standby mode, certain portions of the device when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de-activated. Even if the leakage current is much smaller than the normal operating current of the circuit, the leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest.

To summarize, some performance criteria are considered in the design and evaluation of adder cells, such as leakage power, active power, ground bounce noise and robustness with respect to voltage and transistor scaling as well as varying process and compatibility with surrounding circuitries.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate [5], [6]. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30x increase in gate leakage [7], [8]. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation [9]. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power [10].

Power Gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [11], [12], [13],[14]. This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [15], [16], [17], [18] and further peak of ground bounce noise is possible with proposed novel technique with improved stacking power gating technique. This paper focuses on reducing sub threshold leakage power consumption and ground bounce noise during the sleep to active mode transition. The remainder of this paper is organized as follows. In section II, 90nm low leakage 1 bit CMOS full adder circuit is proposed. In section III, the performance analysis and simulation results of conventional CMOS full adder cell and proposed low leakage 1 bit CMOS full adder cell is explained. Then the paper is summarized in section IV.

II. PROPOSED FULL ADDER CIRCUITS

Recently, power dissipation and signal integrity has become an important concern and considerable emphasis is

978-0-7695-4294-2/10 $26.00 © 2010 IEEE
DOI 10.1109/ISED.2010.41

placed on understanding the sources of power and approaches to dealing with power dissipation [3].

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when we implement by the pass transistor logic [4]. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability [4], [13].

Fig. 1 shows the conventional CMOS 28 transistor adder [12]. This is considered as a Base case throughout this paper. All comparisons are done with Base case.

The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs. Transistor sizes are specified as a ratio of Width/Length (W/L).

The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are proposed in Design1, Design2 and Design2 with stacking power gating targeting the stand by leakage current, and ground bounce noise.

Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with Design 2 with stacking power gating technique.

The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio of 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is 3.1 times that of NMOS in Design1. The sizing of each block is based on the following assumption. Design 1 is considered as individual block as shown in Fig. 3. Each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because subthreshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost.

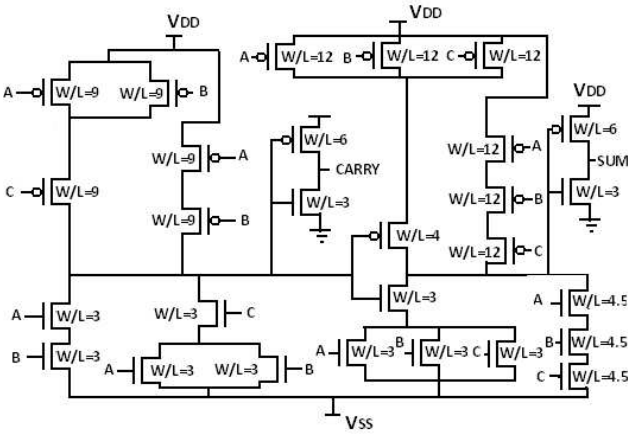

Figure 1. Conventional CMOS full adder.

Modified adder circuit i.e. Design 2 shown in Fig. 4, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The same inverter size has been maintained on each block as shown in the Fig. 5. The goal of this design is to reduce the standby leakage power.

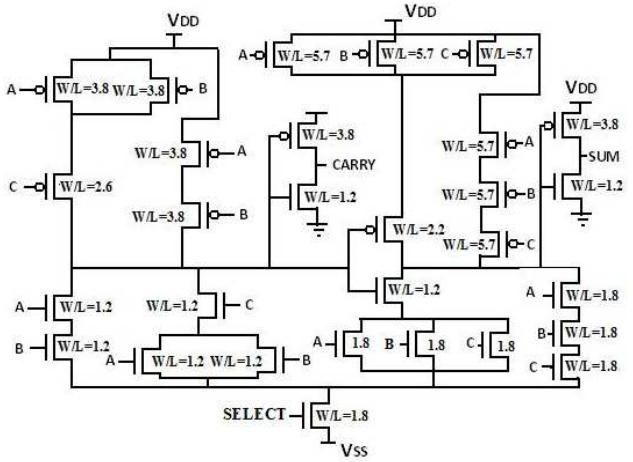

Figure 2. Full adder (Design1) circuit with sleep transistor[18].

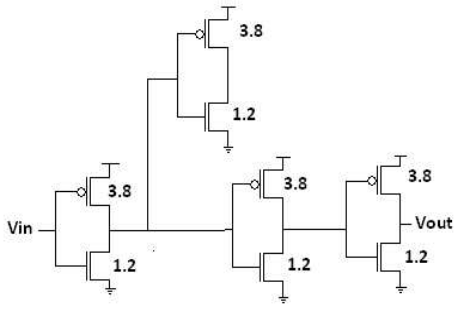

Figure 3. Equivalent circuit for Design1

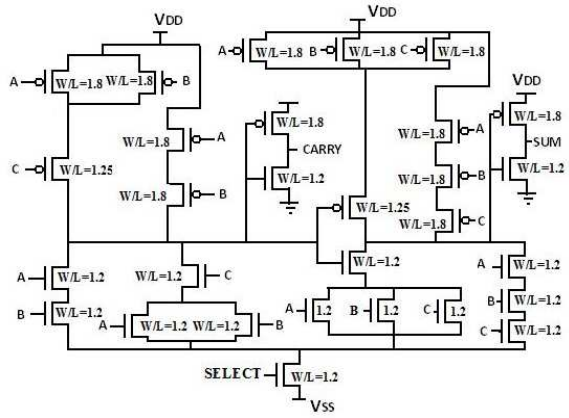

Figure 4. 1 bit full adder (Design2) circuit with sleep transistor[18]

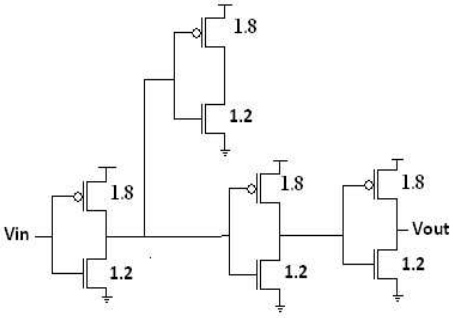

Figure 5. Equivalent circuit for Design2.

Though the given Design1 and Design2 are capable of reducing the ground bounce noise and the leakage current but the reduction in the ground bounce noise is not improved to a significant level in these two designs so there is need of a design which is capable to reduce the ground bounce noise to a significant level without an appreciable increase in leakage current .So here we propose an adder design (figure 6) which is a modification of Design2 using stacking power gating technique[19] . In this technique, stacking sleep transistors are used to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce.

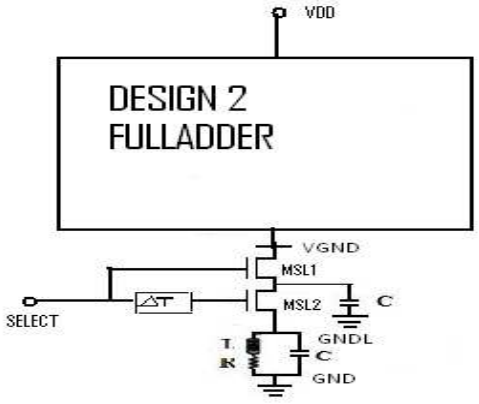

Figure 6. Design 2 with stacking power gating technique (proposed.)
Modified Design 2

In this technique, the leakage current is reduced by the stacking effect, turning both MSL1 and MSL2 sleep transistors off. Here, we apply the SELECT input in a manner by which the ground bounce noise (which is the algebraic summation of ground bounce noise of both the transistor) is minimum. This is achieved by adjusting the value of ΔT (this is the delay introduced to the SELECT signal using delayed buffer) which gives the summation of ground bounce noises of these two transistors minimum. When the value of ΔT is half of the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise superimposes with the negative peak thereby bringing it closer to zero.

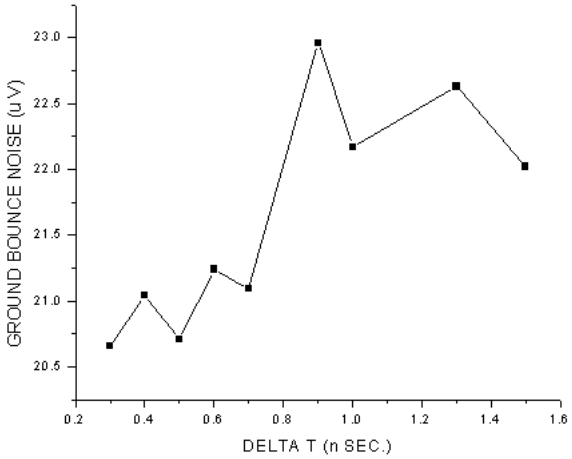

Figure 7.Variation of Ground Bounce Noise with respect to Δ T.

III. Performance Analysis And Simulation Results

We have performed simulations using cadence-spectre simulator and the technology used for simulation is 90nm.

A. Active power

The power dissipated by the circuit when the circuit is in active state. Active power is measured by giving input vectors and calculating the average power dissipation during this time. Considered simulation time to calculate active power is 50ns. Input vectors have been given in such a way that it covers almost all input vector combinations. The same vectors and simulation time has been given to Base case to compare the results. This active power includes dynamic power as well as the static power so it is being named as an active power.

As shown in the Table. I, in case of Design1,Design2 and Design 2 with stacking power gating active power is greatly reduced compared to the Conventional 1 bit full adder cell. This reduction is almost 40.48% , 63.85% and 61.12% in case of Design1,Design2 and Design2 using stacking power gating respectively compared to the Conventional 1 bit full adder cell.

TABLE I.
ACTIVE POWER DISSIPATION OF 1-BIT FULL ADDER CELL

Circuit	Conventional CMOS	Design 1 [18]	Design 2 [18]	Design2 with stacking power gating
Active Power (µw)	3.488	2.076	1.261	1.3559

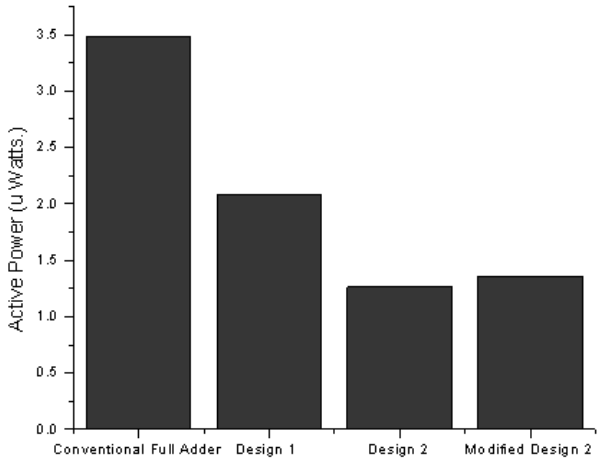

Figure 8. Active power dissipation of 1-bit full adder cell

B. Standby leakage power

Standby leakage power is measured when the circuit is in standby mode. Sleep transistor is connected to the pull down network of 1 bit full adder circuit. Sleep transistor is off by asserting an input 0V. For simplicity, size of a sleep transistor is equal to the size of largest transistor in the network (pull up or pull-down) connected to the sleep transistor. The sleep transistor size in Design1 and Design2 is reduced due to the resizing of the adder cells in proposed circuit. Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design1, Design2 and Design2 with stacking power gating as shown in Fig. 9. In case of Design1 reduction in standby power is about 82%, in Design2 it is about 84% and in Design2 with stacking power gating it is about 87% for all input combinations.

C.Delay

Propagation delay, is the time required for a digital signal to travel from the input(s) of a circuit to the output. The propagation delay for an integrated circuit logic gate may differ for each of the inputs. If all other factors are held constant, the average propagation delay in a logic gate IC increases as the complexity of the internal circuitry increases. The propagation delay is inversely proportional to the speed of the topology and hence is an important performance parameter.

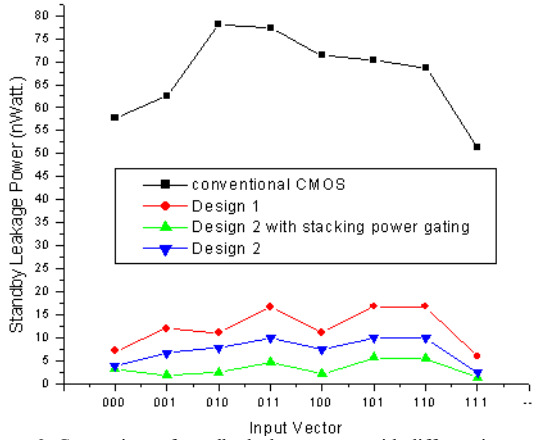

Figure 9. Comparison of standby leakage power with different input combinations of four designs.

Table II comparing the various propagation delays for all the designs and different input combinations is given below. the symbol 'p' is used to denote a pulse input. Here various delay calculated are in pico seconds and (-) sign indicates that the value of sum or carry is same for the given and previous input vector.

TABLE II.
PROPOGATION DELAY OF 1-BIT FULL ADDER CELL

Input Vector			Conventional CMOS		Design1(Psec) [18]		Design 2(Psec) [18]		Modified design2(Psec)	
A	B	C	SUM	CARRY	SUM	CARRY	SUM	CARRY	SUM	CARRY
0	0	p	62.855	-	52.9855	-	59.977	-	59.98	-
0	1	p	99.477	59.201	100.63	60.224	96.857	59.21	96.877	59.213
1	0	p	91.828	56.462	121.505	70.025	113.87	67.394	113.90	67.414
1	1	p	63.017	-	93.845	-	72.086	-	72.109	-
0	P	0	60.289	-	64.119	-	68.087	-	72.692	-
0	P	1	99.378	60.373	97.518	60.061	95.64	60.689	103.59	65.186
1	P	0	97.651	61.575	131.15	74.765	116.22	69.683	108.45	65.218
1	P	1	63.907	-	68.669	-	67.815	-	67.841	-
p	0	0	54.193	-	71.574	-	71.808	-	71.831	-
p	0	1	100.70	57.278	107.05	66.396	102.24	65.6	102.26	65.619
p	1	0	103.96	64.896	122.3	67.369	108.44	64.38	108.59	61.632
p	1	1	66.189	-	63.822	-	62.74	-	62.765	-

D. Ground bounce noise reduction

During the power mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and creates current surges elsewhere, Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these surges result in voltage fluctuations in the power rails. Magnitude of the voltage surge in circuit may erroneously latch to the wrong value or switch at the wrong time. Inductive noise, also known as simultaneous switching noise, is phenomenon that has been traditionally associated with input/output buffers and internal circuitry. Also the noise immunity of a circuit decreases as its supply voltage is reduced. There are some methods such as power gating to address the problem of ground bounce in low-voltage CMOS circuits. The ground bounce model which is used in our simulation is

shown in Fig.10. Ground bounce noise is reduced in all the three designs. Design1, Design2 and Design2 with stacking power gating are compared to the Conventional full adder and is shown in Fig.12.

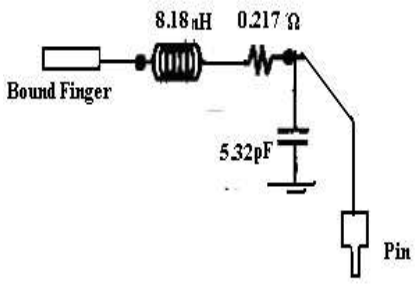

Figure 10. DIP -40 package pin ground bounce noise model [11].

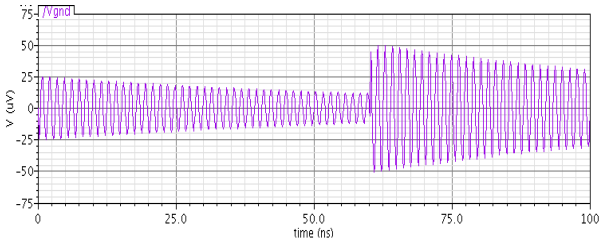

Figure. 11 (a)

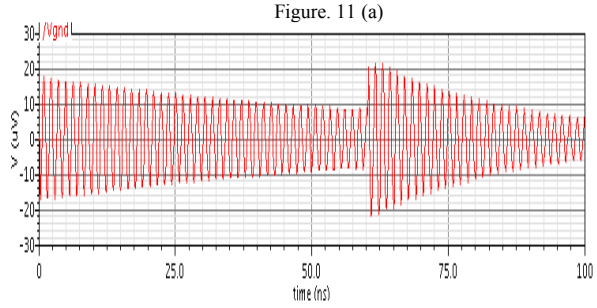

Figure.11 (b)
Waveform showing ground bounce noise in Design2 Fig 11(a) and stacking power gated Design 2 Fig 11(b)

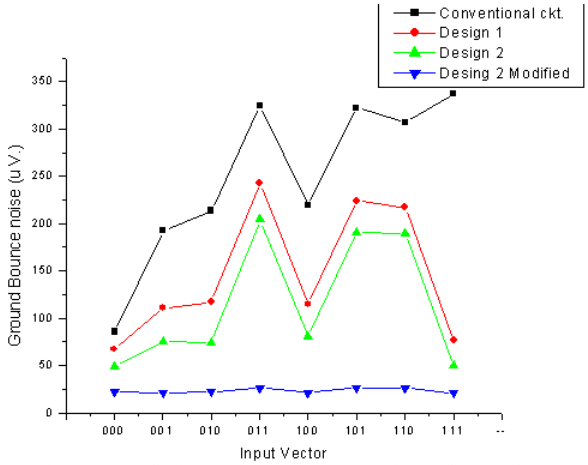

Figure 12. Peak of ground bounce noise graphs for the four designs

IV CONCLUSION

In this paper, Low leakage 1 bit full adder cell is proposed for mobile applications with low ground bounce noise. A high performance stacking power gating structure has been presented which minimizes the ground bounce noise as well as controls the leakage power during the sleep to active mode transition. Stacking power gating technique has been analyzed and the conditions for the important design objectives i.e. (i) Minimum ground bounce noise (ii) Minimum standby leakage power have been achieved by using the modified design where ground bounce noise has been controlled by using stacked sleep transistors with Delta T delayed SELECT signal for MSL2. The leakage power is reduced by 82 % (Design1), 84% (Design2) and 87% (Design2 with stacking power gating) in comparison to the conventional 1 bit full adder cell. Ground bounce noise is reduced about 1.5 times in Design1, 3 times in Design2 and 12.3 times in Design2 with stacking power gating respectively compared to conventional 1 bit full adder cell. Active power is reduced by 40.48% (Design1), 63.38% (Design2) and 61.33% (Design2 with stacking power gating) in comparison to conventional 1 bit full adder cell. The proposed 1-bit full adder cells are designed with 90nm technology and operated with 1V supply voltage.

REFERENCES

[1] Radu Zlatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry- Lookahead Adders With a 240ps 90nm CMOS Design Example," *IEEE J. Solid State circuits*, vol.44, no. 2, pp. 569-583, Feb. 2009.

[2] K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, "Low-Power and High-Performance 1-bit CMOS Full Adder Cell," *Journal of Computers*, Academy Press, vol. 3, no. 2, Feb. 2008.

[3] Rabaey J. M., A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, 2nd Prentice Hall, Englewood Cliffs, NJ, 2002

[4] Pren R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid- State Circuits*, vol. 32, pp. 1079–1090, July 1997.

[5] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006. /

[6] K.Bernstein et al., "Design and CAD challenges in sub-90nm CMOS technologies," *in Proc. int. conf. comput. Aided Des.*,2003, pp.129-136. A. Karnik, "Performance of TCP congestion control with rate feedback: TCP/ABR and rate adaptive TCP/IP," M. Eng. thesis, Indian Institute of Science, Bangalore, India, Jan. 1999.

[7] International Technology Roadmap for Semiconductors," Semiconductor Industry Association, 2005. [Online]. Available: http://public.itrs.net.

[8] H.Felder and J.Ganger,"Full Chip Analysis of Leakage Power Under Process variations, Including Spatial Correlations, "in *proc. DAC*, pp.523-528, June2005.

[9] Jun Cheol Park and Vincent J. Mooney" Sleepy Stack Leakage Reduction" *IEEE transactions on very large scale integration (vlsi) systems*, vol.14, no.1. november 2006.

[10] Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka,"Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating,"*IEEE Transactions on VLSI Systems*,Vol.15, No.11, November2007.

[11] Y.Chang.S.K.Gupta, and M.A.Breuer, "Analysis of ground bounce in deep sub-micron circuits", *in proc.15th IEEE VLSI Test symp.,1997*,pp110-116.

[12] N.West. K.Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley,1993.

[13] Suhwan Kim, Chang Jun Choi, Deog-Kyoon Jeong,Stephen V. Kosonocky, Sung Bae Park," Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures,"*IEEE transactions on Electron Devices*,Vol.55,No.1,January2008.

[14] S.Mutoh et al., "1-v power supply high-speed digital circuit technology with multithreshold-voltage CMOS."*JSSC,* vol.SC- 30, pp.847-854, Aug.1995.

[15] Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, "An effective staggered-phase damping technique for suppressing power-gating resonance noise during mode transition," *10th International Symposium on Quality of Electronic Design*, pp.116-119, 2009.

[16] K. Kawasaki et al., "A sub-us wake-up time power gating technique with bypass power line for rush current support," *IEEE J. Solid-State Circuits* , vol.44, no. 4, pp.146–147, Apr. 2009.

[17] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, " in CCD07, pp. 388-394, 2007.

[18] M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications, " *Proceedings of International Conference on VLSI Design & Communication Systems*, pp.233-238, January 2010.

[19] R.Bhanuprakash, Manisha Pattanaik and S.S.Rajput "Reduction Of Leakage Current And Ground Bounce Noise Using High Performance Stacking Power Gating Logic Circuits, "*proceedings of IEEE TENCON Singapur,pp 1-6,2009.*