# Design of Low Power Logic Gates by Using 32nm and 16nm FinFET Technology

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***Abstract*— In today's world different technologies are present in case of electronics market. The electronics market grown very rapidly because of most of the devices are compact, innovative, giving more efficiency and consumes less power with very small supply voltage. Because of the advancement in the semiconductor technology, integration of whole electronics system on a single chip is practicable. We have seen the change in the semiconductor technology from personal computer to the laptops and then to the cell phones and thus the mobile and computing markets are continue to innovate at dramatic rate. For all this, the most viable successor is a CMOS technology. But the 22nm node of CMOS fails to perform these operations because the shrinking of this CMOS leads to the short channel effect. Multigate FET technology is the most feasible successor to planar CMOS technology at the 22-nm node and beyond. These multi-gate transistors are called fin field-effect transistors (FinFET). Design of NOR and NAND circuits is present in this paper, to improve the speed and power of these gates. Also in this paper, the comparative study of different performance parameters for CMOS and FinFET technology for basic logic gates is present. Dynamic power, current, static power are some parameters which are evaluated with the help of tanner EDA tool.**

***Index Terms*—CMOS, Current, Dynamic Power, NAND, NOR, Static Power, FinFETs, Multigate device and Predictive Technology Model (PTM).**

## I. INTRODUCTION

Today there are an escalating number of portable applications with limited amount of power available, requiring small area, and low-power and high throughput circuitry. For examples all the electronics devices that we use in our daily life like as mobile phones, computers, Televisions, different cars, washing machines, refrigerators, micro ovens and almost all electronics devices. Also for the smart cards, credit cards or a debit cards requires low power [1]-[2]. All of these equipment's have one thing is common, all of these are having one or more semiconductor chips, which are also called as integrated circuits (IC). These ICs are made up of millions of transistors which are etched on the small piece of doped silicon layer with proper interconnections in between them is depending upon the desired functionality. In old days the vaccume tube is used as a transistor, so the size of the device is increases. Also the power and current requires for the vaccume tube is greater than that of transistor [3]-[4]. Therefore the technology and tools available in that time are more complex and difficult to understand. Today the technology has been advance; we can now fabricate millions of transistor in a unit square inch piece of silicon and the technology popularly known as Very Large Scale Integration (VLSI). Therefore circuits which are consuming the low power become major concern factor for designing of microprocessors and system components. The research effort in low power microelectronics has been intensified and low power VLSI systems have emerged as exceedingly in demand.

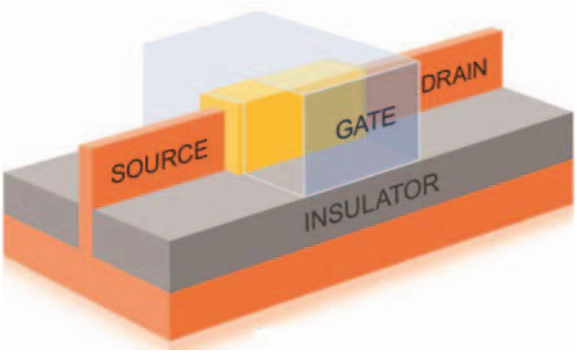
The organization of the paper is in the following way where section II reviews brief study of FinFET technology and its simulation methods. Section III describes the different designing of CMOS circuits and its analysis, section IV evaluates the performance and results of proposed system and finally the section V concludes this paper.

## II. BASICS OF FINFET

The name FinFET is given to this technology because the FET structure used in this looks like a set of fins when viewed. The FinFET transistors are employed on a single gate which is stacked on the top of two vertical gates and it allows three times more the surface area for electrons to travels. Figure 1 shows the 3D view of FinFET. This figure shows the construction of FinFET transistor [5].

The planer transistor scaling in deep-sub micrometer CMOS technology that has been approached its limits up to sub-22-nm nodes, therefore it has owing to very less electrostatic integrity, which is detected as a degraded short-channel behavior and high leakage current [6]-[7]. These problems can be overcome by using Multi-gate field-effect transistors (FETs) because it has higher control of the channel potential than the multiple gates wrapped around the body. Among the multigate FETs, the FinFETs/Ω-FETs have emerged as a best option to turn on the device and is used to provide the maximum gate drive. The back-gate bias is used to alter the threshold voltage ($V_{th}$) of the front gate this is also used to control the OFF-current ($I_{OFF}$) of the semiconductor device.

$I_{OFF}$ current in SG-mode devices is generally much higher than the IG-mode devices with a back gate held an above or below the rail for the p-type or n-type material and because of the fixed $V_{th}$, it cannot be altered electrically [8]-[9].



Fig,1. 3D FinFET.

The IG mode devices provides the advantage of controlling the device voltage $V_{th}$, and the delay/leakage current of device, but the IG mode of operation uses complicated transistor layout strategy. The multifin IG-mode FinFETs used to provide larger spacing between the source and drain regions, as well as it has larger fin pitch in order to land a contact to the back gate in comparison to corresponding multifin SG-mode FinFETs with compact layouts. The main design aim for very-large-scale integration (VLSI) designers is to meet performance requirements within a specific power budget. So, power efficiency has implicitly increased importance [10]. This paper work explores how the circuits based on FinFETs, which is an the emerging transistor technology that is to be likely to enhance or replace bulk CMOS at 22-nm and beyond, offer interesting power tradeoffs. Also we compare the CMOS based FinFET circuits using PTM models under 32nm and 16nm node. While some of the works have been proposed earlier, to our knowledge, this is the first time we are doing a comparison between different technology nodes in Tanner EDA tool.

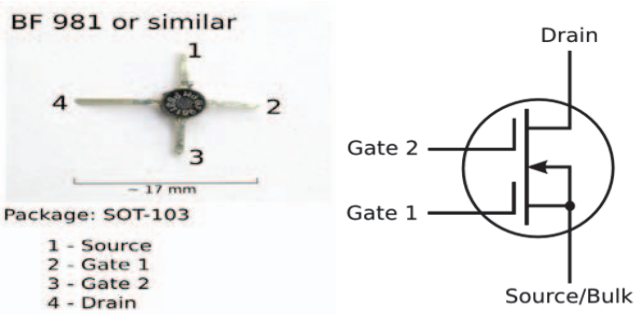


Fig.2. FinFET Symbol.

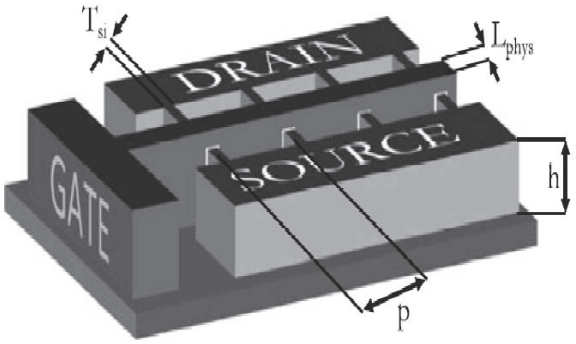


Fig.3. Multi Fin FinFET

In this paper we simulate the different logic gates (NAND, NOR) using FinFET PTM models to provide a low power designs. Figure 2 shows the FinFET Symbol.

The multiple FinFET are connected together on a single chip called multi-fin FinFET. Figure 3 shows the multi-fin FinFET. It consists of the thin silicon body which thickness is denoted by $T_{Si}$ and wrapped by gate the electrodes. The current flow in FinFET is parallel to the wafer plane, whereas the channel is perpendicular to the plane of a wafer. Due to this reason, the device is termed as quasi-planar. The independent control of a front and back gates of the FinFET is obtained by etching away the gate electrode at a top of the channel. The effective gate width of the FinFET is 2nh, where n is a number of fins and h is a fin height. Therefore, the wider transistors with higher currents are obtained by using the multiple fins. And the fin pitch *(p)* is a minimum pitch between adjacent fins allowed by lithography at a particular technology node. By using spacer lithography, *p* can be made as small as half of the lithography pitch. The FinFETs have been used in variety of digital and analog circuits. Uptill now simulation of CMOS and FinFET have been done under 32 nm process technology. In this paper work we have simulated and compared both CMOS and FinFET logic gates under 32nm. Again the result of the 32nm FinFET has been compared with the 16nm FinFET logic gates [11]-[12]. Power consumption in 32nm FinFET is less compared to the 32nm CMOS logic gates. For simulation purpose the Predictive Technology Model (PTM), it provides predictive, customizable, and accurate model files for the future transistor and it also interconnect the various technologies. All of these predictive model files are compatible to the standard circuit simulators, like as SPICE, and scalable with the wide range of process variations. As an evolution of previous Berkeley Predictive Technology Model (BPTM), the PTM will provides the following novel features for robust design exploration toward the 10nm:

- The predictions of various transistor structures, such as ultra-thin-body SOI, FinFET (double-gate) and bulk for sub-45nm technology nodes.
- It is a new methodology of the prediction, which is more continuous, scalable, and physical over the technology generations.
- The predictive models for emerging variability and reliability issues such as NBTI.

## III. The CMOS Design And Analysis

This section describes the proposed simulation of gates scheme. The simulation of the NAND gate and the NOR gate is done with the help of PTM models.

Logic gates are the elementary building blocks of any logic circuits. Also the NAND and NOR are the universal gates from which we can design any logic gates. In this paper low power NAND and NOR logic gates are design [13]. The NAND gate is also called as NOT AND gives output high only when it's one of the input is low and when both the input is high output is low. Figure 4 shows the conventional NAND gate symbol. Figure 5 shows the NAND gate design using CMOS and Table I shows the truth table for the NAND gate.

The NOR gate is also called as NOT OR gives output high only when it's both the input is low and when one of or both the input is high output is low.

The figure 6 shows the conventional NOR gate symbol. Figure 7 shows the NOR gate design using CMOS and Table II shows the truth table for the NOR gate. Where the *A* and *B* are the inputs are applied to the gate and *Y* represents the output of gate [14]-15].

In this paper different logic gates such as NAND, NOR in CMOS technology as well as in FinFET technology under 32nm by using Tanner EDA tool with spice models are simulated. The experimental results are compared with different parameters such as dynamic power, static power etc.

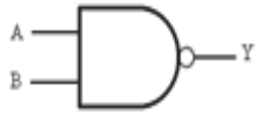



Fig.4.NAND Gate Symbol.

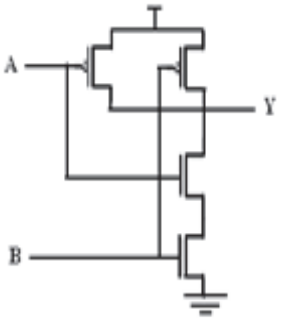



Fig.5. NAND Gate design using CMOS.

TABLE I. TRUTH TABLE FOR NAND GATE

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |


Fig.6.NOR Gate Symbol.

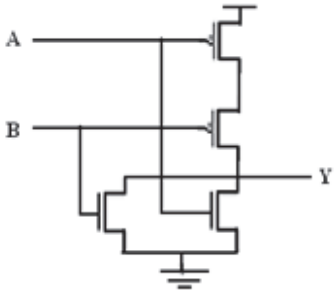



Fig.7. NOR Gate design using CMOS.

TABLE II. TRUTH TABLE FOR NOR GATE

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## IV. EXPERIMENTAL RESULTS

This section describes the proposed simulation of experimental results of different gates and the experimental results which are obtained are compared with different parameters such as dynamic power, static power etc.

Figure 8 shows the simulation results of NAND gate, from that figure it is clear that the simulation results are verified that are presents in table1. Figure 9 shows the simulation graph of dynamic switching power for the 32nm CMOS technology while Figure 10 shows the simulation graph of dynamic switching power for proposed 32nm FinFET method.

Figure 11 shows the simulation graph of dynamic switching power for proposed 16nm FinFET method.

From these simulation results it is clear that the dynamic switching power by using proposed FinFET method is less than the CMOS technology.

Similarly, figure 12 shows the simulation result of NOR gate, from that figure it is clear that the simulation results are verified that are presents in table1.

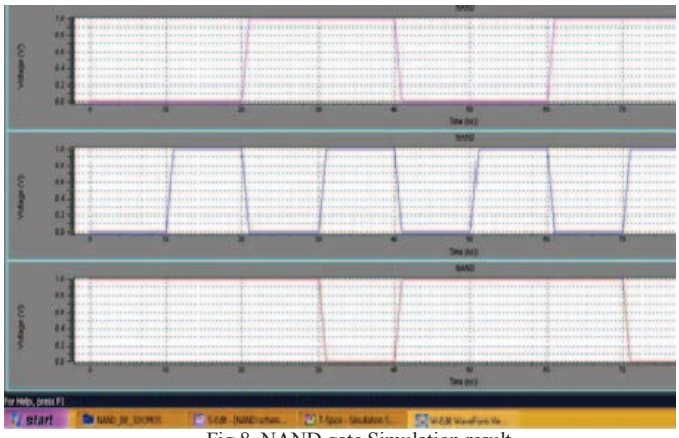


Fig.8. NAND gate Simulation result

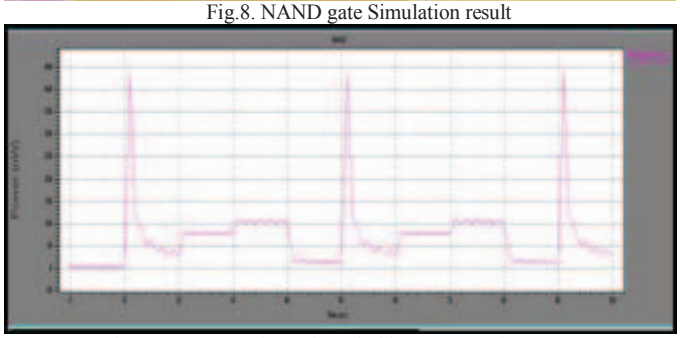


Fig.9. CMOS_32 dynamic(switching) power of NAND gate.

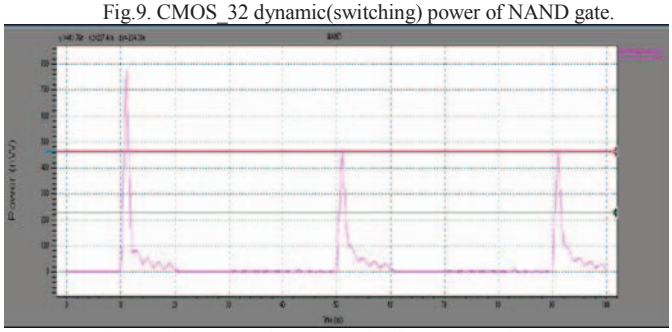


Fig.10. FinFET_32 dynamic(switching) power of NAND gate.

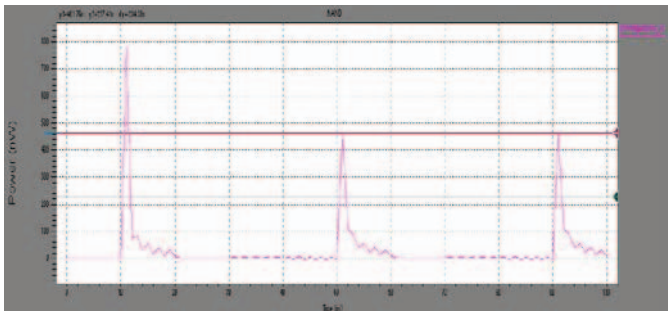


Fig.11. FinFET_16 dynamic (switching) power of NAND gate.

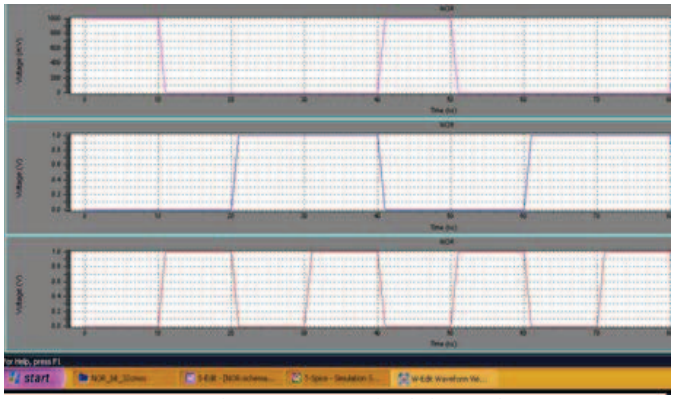


Fig.12. NOR gate Simulation result

Figure 13 shows the simulation graph of dynamic switching power for the 32nm CMOS technology while Figure 14 shows the simulation graph of dynamic switching powers for proposed 32nm FinFET method. And figure 15 shows the simulation graph of dynamic switching power for proposed 16nm FinFET method for NOR gate.

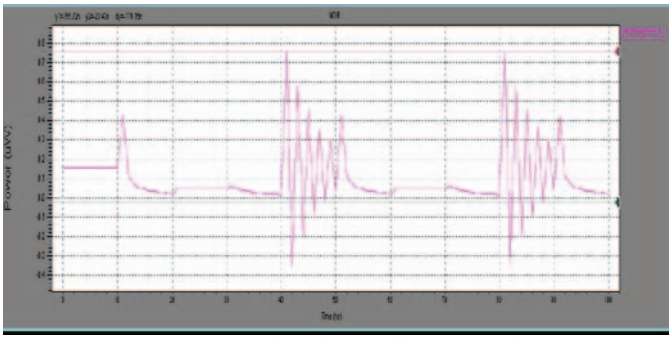


Fig.13. CMOS_32 dynamic (switching) power of NOR gate.

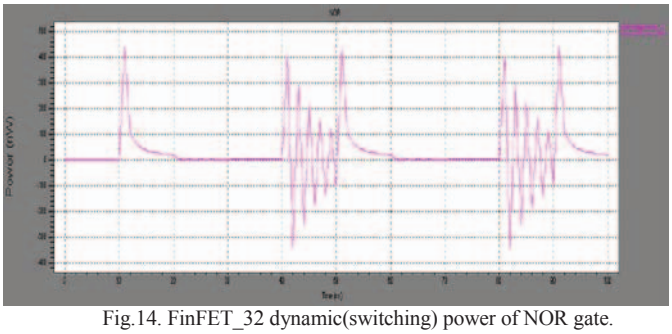


Fig.14. FinFET_32 dynamic(switching) power of NOR gate.

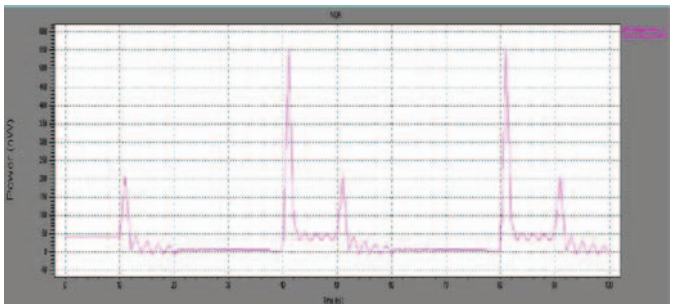


Fig.15. FinFET_16 dynamic (switching) power of NOR gate.

Also from these simulation results it is clear that the dynamic switching power by using proposed FinFET method is less than the CMOS technology.

We simulate both gates using Predictive Technology Models (PTM) for 32nm CMOS, 32nm FinFET and 16nm FinFET. As the manufacturing processes of the FinFET are similar to the CMOS, we simulate the CMOS designs for FinFET models. Simulated result of the gates confirms the optimization of the power dissipation almost 20% less than the CMOS technology at 0.8v. We can decrease the supply voltage to 0.7v to optimize the power but there are fluctuations in the output of the gates. For proper operation of the gate we have given 0.8 supply voltage. Simulation results are measured using Tanner EDA tool 13.0. The simulation results for NAND gate are summarized in table III. From that table it is clear that the power and current required for NAND gate by using FinFET is less than the CMOS technology.

TABLE III. SUMMARY OF SIMULATION RESULT FOR 32NM CMOS AND FINFET FOR NAND GATE.

| **Parameters** | **CMOS** | **FinFET** |
|---|---|---|
| Technology used | 32 | 32 |
| Voltage | 0.8 v | 0.8 v |
| Dynamic Power | 461.79 nw | 438.61 nw |
| Static Power | 3.059 nw | 211.54 pw |
| Current | 3.824 nA | 264.42 pA |

TABLE IV. SUMMARY OF SIMULATION RESULT FOR 32NM CMOS AND FINFET FOR NOR GATE.

| **Parameters** | **CMOS** | **FinFET** |
|---|---|---|
| Technology used | 32 | 32 |
| Volatge | 0.8 v | 0.8 v |
| Dynamic Power | 7 µw | 439.99 nw |
| Static Power | 156.93 nw | 1.58 nw |
| Current | 196.16 nA | 1.98 nA |

In this paper we have also simulated 32nm FinFET and 16nm FinFET. The simulation results are summarized in table IV. In this we have seen that power is optimized near about 95%. We know that if the technology node decreases the no. of transistor count on the die gets double on the same chip area. Therefore, here we can say that area is optimized 50%.

The comparisons of different parameters of 32nm FinFET and 16nm FinFET are shown in table V.

TABLE V. SUMMERY OF SIMULATION RESULT FOR BOTH FINFET BASED GATES UNDER 32NM AND 16NM.

| **Parameters** | **FinFET** | | **FinFET** | |
|---|---|---|---|---|
| Technology used | 32 | | 16 | |
| Gates | NAND | NOR | NAND | NOR |
| Voltage | 0.8 | 0.8 | 0.3 | 0.3 |
| Dynamic Power | 438.61 nw | 439.99 nw | 187.30 nw | 200 nw |
| Static Power | 211.54 pw | 1.58 nw | 3.37nw | 42.47 nw |
| Current | 264.42 pA | 1.98 nA | 11.24nA | 141.59nA |

## V. CONCLUSION

The proposed method can be used in number of portable electronics devices applications which requires limited amount of power. This scheme is effective to reduce the power and current of logic gates. This study also shows different considerations for designing different logic gates. The current system can survive in different electronics devices for long period. Due to the use of these components the size of device is to be reduces. The device performance and parameters such as dynamic power, static power, current, simulation time of NAND and NOR gate under 32nm and 16nm are simulated and evaluated using Tanner EDA Tool 13.0 version using PTM spice models. We have observed that power and area is optimized under 32 and 16nm technology node.

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