FinFET Based 4-BIT Input XOR/XNOR Logic Circuit

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***Abstract* –In this paper a structure for direct 4-BIT XOR/XNOR logic cell is proposed. This structure is proposed using pass transistor logic with FinFETs. This structure has less delay for the reason that its critical path consists of a minimum number of transistors. The basic advantage of this circuit is their symmetry in the logic. This design has a full voltage swing at the outputs and hence it has the good driving capability. The proposed design produces perfect outputs, even at low voltages and at high frequencies with the lesser transistor count. The proposed design is simulated using Cadence 20 nm FinFET technology at various supply voltages assorting from +0.6 V to +0.9 V. The simulation results illustrate that the proposed design has less delay and as well as less power consumption.**

Keywords- Driving capability; 4-BIT input XOR logic; 4-BIT input XNOR logic; Full Swing; Low Power; Pass Transistor Logic (PTL); FinFET

I. INTRODUCTION

The primary impediments of CMOS technology in sub micron/threshold region are high sub-threshold and gate dielectric leakage currents. To overcome these problems the double gate FinFET devices are the substitutes. It has lower gate leakage, stronger gate control and the ability to reduce short channel effects. Due to these superior characteristics FinFET device is found advantageous in terms of speed, sizing of transistors and performance in sub- micron/threshold regions. Top view of the double gate FinFET structure [1] and its symbol are shown in Fig. 1. The FinFET presents the double-gate silicon-on-insulator device, one among geometries being introduced to avoid the effects of short channels and mitigate drain-induced barrier lowering. A narrow channel placed between source and drain is named as "fin". A thin insulating oxide layer on either side of the fin isolates it from the gate. FinFETs with a thick oxide on top of the fin are called double-gate FinFETs. In gain to having excellent channel control, the FinFET transistors are also offered approximately twice the on-current compared to the planar MOSFETs because of the dual gates, yet without increasing channel doping. This is one of the major advantages for the carrier mobility and results in a low gate leakage simultaneously. All drawbacks should overcome by these types of FinFET devices and also it is suitable for emerging nano scale device technologies. To design a low power, efficient complex circuit, it is more flexible and easy to use FinFETs with independent gates [2]. At low $+V_{dd}$ value the FinFET provide higher drive currents and lower flicker noise levels, it is suitable for analog and digital applications [3].

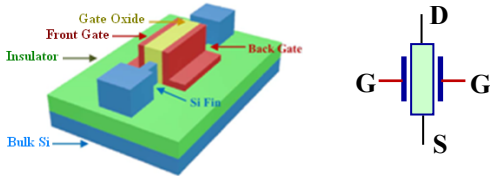

Figure 1. (a) Top view of double gate FinFET structure and (b) its symbol.

In recent years, there has been an enormous gain in the use of electrical and electronic equipment in the biomedical field for the clinical and research functions. Many types of instrumentation systems are applied in hospitals for diagnostic and remedial uses. For example, to measure and process the human blood parameters like glucose, blood pressure, oxygen etc the electronic arithmetic circuitry is used. The glucose levels are normally in the range of 70 to 120 mg/dL, normal blood pressure is 120/80 and oxygen saturation value is approximately 75 to 99 %. And the human body temperature (98.6°F) is also measured with these arithmetic circuits using sensors. The demand for low voltage/low power circuits are increased in the biomedical instrumentation systems [4]-[10].

With the advent of portability the need for low power and high performance circuits have been increasing significantly. Many of the low power circuits use XOR/XNOR logic gates as one of the basic blocks of the applications such as full adder, parity checker, multiplier, comparator and in error control encoders and decoders [11]-[26]. Hence it is used extensively in many VLSI systems as a part of the critical path that determines the overall performance of the system. So enhancing the performance of the XOR and XNOR gates plays an important role.

In this paper a low voltage operated FinFET based direct 4-bit XOR/XNOR circuit is proposed which is found more suitable for the stated biomedical applications. The proposed structure can be extended for 8-bit, 16 bit etc. The proposed structure has high operating speed at low voltages and this proposed FinFET device XOR/XNOR cells work at sub-micron region with less leakage currents.

The remaining section of the paper is organized as follows. In section II, proposed 4 and 8 BIT input XOR/XNOR structure implementation is briefly stated and section III explains simulation results and finally section IV conclude the paper.

II. PROPOSED 4-BIT AND 8-BIT INPUT XOR/XNOR STRUCTURES

In futuristic portable devices, the supply voltage is decreased to bring down the power dissipation. As the supply voltage is scaled down below the threshold voltage, the normal MOSFET device cannot be used due to lower I_{ON}/I_{OFF} ratio which may however reduce the static power dissipation. The power consumption becomes a major setback for further scaling. The continued reduction of MOSFET size is contributing to increased leakage current due to short channel effects. A promising alternative for MOSFET which does not suffer from these limitations is FinFET. FinFET is used as an substitute for low power applications due to its higher sub threshold swing, extremely low off state current (I_{OFF}) and excellent sub-threshold characteristics. Hence FinFET transistor has invited a lot of attention for analog and RF applications. Also the dynamic power dissipation will get decreased in FinFET since the operating voltage is very low.

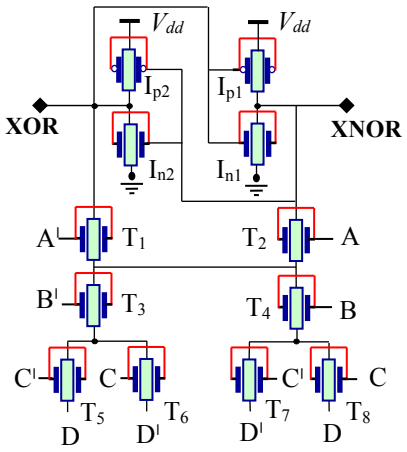

Figure 2. Proposed structure for 4-BIT input XOR/XNOR circuit

The proposed structure of 4-BIT input XOR/XNOR is shown in Fig. 2. This structure is constructed using Pass Transistor Logic (PTL) and two inverters. In Fig. 2, the logic is implemented with n-FinFET transistors and it requires complementary input signals. The proposed structure is symmetric and simple. All the inputs except the least significant input acts as control signals and the least significant input and/or the complementary of this least significant input is passed to the outputs. The back to back connection of these two inverters acts as restoration logic to get a full swing since the pass transistor logic has the threshold voltage loss problem. In any digital system, when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state is called meta-stability [27]. In the proposed Fig. 2 and Fig. 3 structures the probability of an inverter (consists of FinFETs I_{p1}-I_{n1}) and inverter (consists of FinFETs I_{p2}-I_{n2}) coming out of metastabilty increases exponentially with time.

In Fig. 2, logic is constructed using 8 n-FinFET transistors and two inverters. The working of the proposed 4 input XOR/XNOR structure can be better analyzed by considering the complete set of input signals ABCD = 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111.

For example, in Fig. 2, for '0000' combination of inputs the transistors T_1, T_3 and T_5 are switched ON so that the full logic '0' i.e. input D is passed to XOR output and full logic '1' is produced at the XNOR output through the inverterI_1. When an input pattern is '0001', the transistors T_1, T_3 and T_5 are switched ON so that degraded logic '1' is generated at XOR output, then the transistors in the inverters I_{n1} and I_{p2} forms, feedback loop to produce full logics at the both XOR and XNOR outputs. For ABCD = '1101', then the transistors T_2, T_4 and T_7 are switched ON and input D^I i.e. full logic '0' is passed to the output of XNOR and full logic '1' is generated at the output XOR through inverter I_2. For ABCD = '1100', then the transistors T_2, T_4 and T_7 are switched ON and input D^I i.e the degraded logic '1' is passed to the output of XNOR then the transistors in the inverters I_{n2} and I_{p1} forms a feedback loop to produce full logics at both XOR and XNOR outputs. A similar operation applies to the rest of the cases.

Fig. 3 shows the extended structure of Fig. 2 for 8-BIT input XOR/XNOR logic circuit. Fig. 3 operation is similar to the structure in Fig. 2 which is already presented, so that they are not included here to avoid repetition and also simulation results.

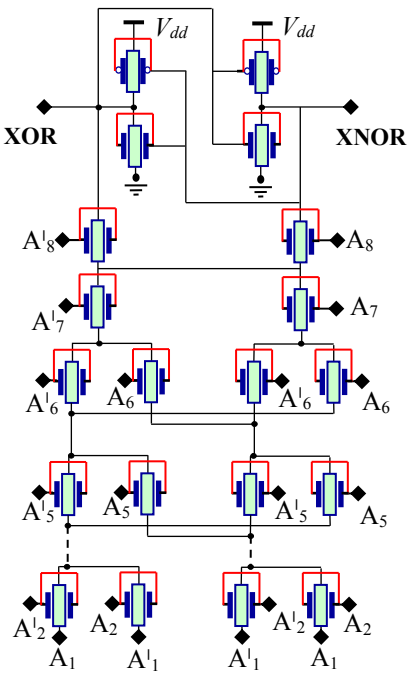

Figure 3. Structure for 8-BIT input XOR/XNOR circuit

III. Simulation Results

Four BIT input XOR/XNOR circuit shown Fig. 2 was simulated using Cadence 20 nm FinFET technology at various supply rail voltages from +0.6 V to +0.9 V. Simulations were carried out to exhibit the effect of different supply rail voltages to the output swing of the proposed Fig 2. Here the transient response of Fig. 2 is shown at the voltage of +0.6 V in Fig. 4. From the Fig. 4 it is to be noted that the proposed circuit is giving full swing operation. Table 1 shows the transistor count for different circuits of proposed structure and cascaded structures. When compared to cascaded circuits the proposed structure takes less number of transistors. Fig. 2 circuit's propagation delay and dynamic power dissipation are shown in Fig. 5 and Fig. 6 respectively.

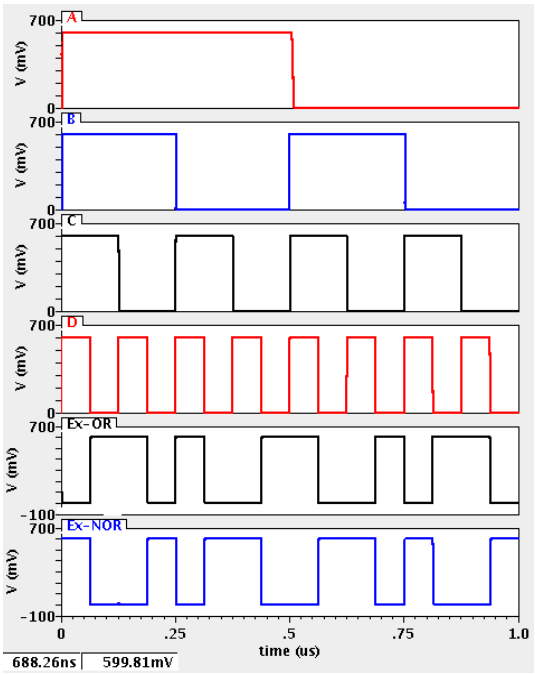

Figure 4. Input and output waveforms of 4-input XOR/XNOR Circuit

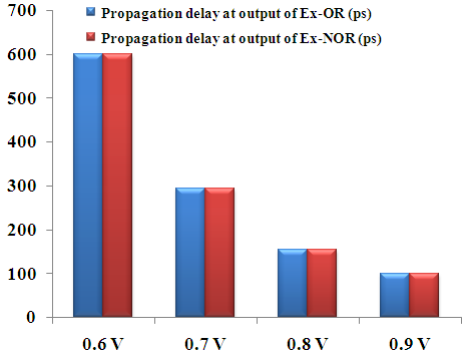

Figure 5. Simulated propagation delay Vs Voltage

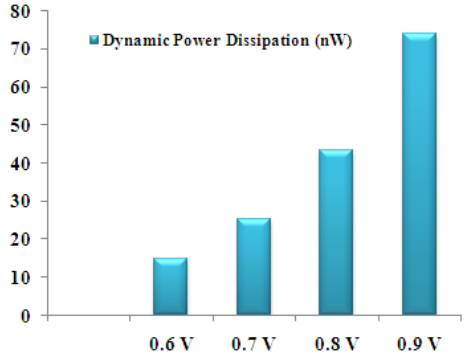

Figure 6. Simulated dynamic power dissipation Vs Voltage.

TABLE I. Comparative Transistor Count Of Candidate Designs

S.No	Fan-in of XOR/ XNOR Circuit	No. of transistors	By cascading of 2 input XOR/XNOR gates No. of transistors [ref]
1.	4	20 [Fig. 2]	30 [11], 24 [12], 36 [13], 30 [13], 42 [13], 30 [14]
2.	8	44 [Fig. 3]	70 [11], 56 [12], 84 [13], 70 [13], 98 [13], 70 [14]

IV. Conclusion

The proposed structure for 4-BIT input XOR/XNOR circuit is symmetric and simple. This structure is proposed using pass transistor logic with FinFETs. This structure has less delay for the reason that its critical path consists of a minimum number of transistors. The basic advantage of these circuits is that their symmetry in the logic makes them easy to layout. The proposed design produces perfect outputs, even at low voltages and at high frequencies with the lesser transistor count. The new design structure was simulated using Cadence 20 nm FinFET technology with a supply rail voltage ranging from +0.6 V to +0.9 V. The simulation results illustrate that the proposed design has less delay as well as less power consumption.

References

[1] Xue Lin, Yanzhi Wang and Massoud Pedram, "Stack sizing analysis and optimization for FinFET logic cells and circuits operating in the sub/near-threshold regime", *in Proc. IEEE 15th International Symposium on Quality Electronic Design*, pp. 341-348, 2014.

[2] V. Lavanya, S. S. Kumar, L. Bhagyalakshmi, "RF harvesting and its applications in low power devices," presented at the *IEEE International Conference on Advanced Computing*, Chennai, India, Dec. 17-19, 2015.

[3] H. Lui, S. Datta, V. Narayanan, "Steep switching tunnel FET: A promise to extend the energy efficient road map for post CMOS digital and analog/RF applications," *International Symposium on Low power electronics and design*, Beijing, China, Sept. 4-6, 2013.

[4] C. S. Kumar, K. I. Ramachandran and A. A. Kumar, "Vital sign normalisation for improving performance of multi-parameter patient monitors", *Electronics Letters,* vol. 51, issue. 25, pp. 2089-2090, 2015. DOI: 10.1049/el.2015.2636.

[5] A. M. Nia, M. Mozaffari-Kermani, S. Sur-Kolay, A. Raghunathan and N. K. Jha, "Energy-efficient long-term continuous personal health monitoring", *IEEE Transactions on Multi-Scale Computing Systems,* vol. 1, no. 2, pp. 85-98, 2015. DOI: 10.1109/TMSCS.2015.2494021.

[6] M. K. Chaithanya, K. V. K. Kishore and Avireni Srinivasulu, "Continuous blood pressure measurement and data logging device with SMS alerts", *International Journal of Multimedia and Ubiquitous Engineering*, vol. 9, no. 8, pp. 25-38, 2014.

[7] M. S. Akbar, H. Yu and S. Cang, "A holistic simulation model for remote patient monitoring systems using Wireless Body Area Sensor Networks (WBASNs)", in Proc. *International Conference on Software, Knowledge, Information Management and Applications* (SKIMA), Kathmandu, Nepal, 15-17 Dec. 2015, pp. 1-5. DOI: 10.1109/SKIMA.2015.7399990.

[8] X. Luo, L. Wang and L. Yang, "Effects of rapid ascent to high altitude on vascular tone", in Proc. *International Conference on Information Technology in Medicine and Education* (ITME), Huangshan, China, 13-15 Nov. 2015, pp. 103-107. DOI: 10.1109/ITME.2015.79

[9] T. Y. Abay and P. A. Kyriacou, "Accuracy of reflectance photoplethysmography on detecting cuff-induced vascular occlusions", in Proc. *37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society* (EMBC), Milan, 25-29 Aug. 2015, pp. 861-864. DOI: 10.1109/EMBC.2015.7318498

[10] M. K. Chaithanya, A. Srinivasulu and K. V. K. Kishore, "Blood pressure measurement and data storing using volume compensation method", *in proceedings of the IEEE International Conference on Devices, Circuits and Communications* (IEEE ICDCCom-2014), Mesra, India, Sep 12-13, 2014. DOI: 10.1109/ICDCCom.2014.7024700.

[11] A.M. Shams, T.K.Darwish and M.A.Bayoumi, "Performance analysis of low power 1-bit CMOS full adder cells," *IEEE Transactions on VLSI systems*, vol.10, no.1, pp 20-29, 2002.

[12] M. A. Elgamel, S. Goel, and M. A. Bayoumi, "Noise tolerant low voltage XOR-XNOR for fast arithmetic ", *Great Lake Sym. VLSI, Washington DC*, pp. 285-288, April. 28-29, 2003.

[13] S. Geol, M. E. Elgamel, M. A. Bayouni and Y. Hanafy, "Design Methodologies for high-performance Noise-tolerant XOR-XNOR Circuits", *IEEE Trans. Circuits and Sys. - I*, vol. 53, no. 4, 2006.

[14] Sarada Musala and B. R. Reddy, "Implementation of a Full Adder Circuit with New Full Swing Ex-OR/Ex-NOR Gate" *IEEE Conference-Prime Asia*, pp. 29-33, Dec. 19-21, 2013.

[15] S. S. Mishra, S. Wairya, K. Nagaria and S. Tiwari, "New design methodologies for high speed low power XOR-XNOR Circuits" *World Academy of Science, Engineering and Technology*, pp. 196-202, 2009.

[16] Rajeev Kumar and Vimal Kant Pandey, "A New 5-Transistor XOR-XNOR circuit based on the pass transistor logic*," IEEE World Congress on Information and Communication Technologies*, pp. 667 – 671, Dec 10- 11, 2011.

[17] A. Srinivasulu and Sivadasan. K, "Optical Exclusive-OR Gate", *Journal of Microwaves, Optoelectronics and Electromagnetic Applications,* vol. 3, no. 1, pp. 20-25, 2003. ISSN: 1516-7399, ISSN: 2179-1074.

[18] Nabihah Ahmad and Rezaul Hasan, "A 0.8V 0.23 nW 1.5 nS Full Swing Pass Transistor XOR gate in 130nm CMOS," *Active and Passive Electronic Components*, vol. 2013, Article ID 148518, 6 pages, 2013. doi:10.1155/2013/148518.

[19] Pedro Reviriego, Salvatore Pontarelli, Juan Antonio Maestro and Marco Ottavi, "A method to construct low delay single error correction codes for protecting data bits only" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 3, pp.479-483, 2013.

[20] D. Radhakrishnan, "Low voltage low power CMOS full adder," *IEE Proc.-Circuits, Devices and Systems*, vol. 148, no. 1, pp. 19-24, 2001.

[21] Avireni Srinivasulu and M. Rajesh, "ULPD and CPTL pull-up stages for differential cascode voltage switch logic," *Journal of Engineering,* Vol. 2013, Article ID 595296, 5 pages, 2013.

[22] Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, A System Perspective, *Pearson Edition Asia*, 2nd Ed, pp. 304-305, 2004.

[23] U. Ko, P. T. Balsara and W. Lee, "Low-power design techniques for high-performance CMOS adders," *IEEE Trans. Very Large Scale Integr. Syst.,* vol. 3, pp. 327-333, 1995.

[24] W. Jyh-Ming, F. Sung-Chuan and F. Wu-Shiung, "New efficient designs for XOR and XNOR functions on the transistor level," *IEEE Journal of Solid- State Circuits*, vol. 29, pp. 780-786, 1994.

[25] Reto Zimmermann and Wolfgang Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", *IEEE Journal of Solid State Circuits*, vol.32, no.7, pp.1-12, 1997.

[26] T. V. Rao and A. Sinivasulu, "Modified level restorers using current sink and current source inverter structures for BBL-PT full adder", *Radioengineering*, Vol. 21, no. 4, pp.1279-1286, 2012.

[27] www.cs.ucr.edu/~ehwang/courses/cs120b/flipflops.pdf