Ultra Low-Power High-Speed Single-Bit Hybrid Full Adder Circuit

Manoj Kumar[1],
M.Tech VLSI & Embedded System Design,
Department of ECE,
Maulana Azad National Institute of Technology,
Bhopal, India.
E-mail: ermk1592@gmail.com

R.K Baghel[2],
Professor,
Department of ECE,
Maulana Azad National Institute of Technology,
Bhopal, India.
E-mail: rakbagh@yahoo.co.in

***Abstract*—In this paper a low power hybrid 1-bit full adder circuit is designed and extended for 4 bit ripple carry adder (RCA). A new XNOR logic is designed using complimentary-metal-oxide semiconductor (CMOS) logic and Pass transistor logic. CMOS weak inverters improve the power consumption while pass transistors overcome voltage degradation problem. Carry logic is designed using transmission gates which reduces the carry propagation path. A 4-Bit RCA is also designed using the proposed single bit full adder. The proposed full adder and RCA are designed in 180nm technology and post layout simulations are done using Cadence Virtuoso. Power, delay, power delay product (PDP) and area are performance parameters of the proposed full adder which are calculated using *umc* technology. The power and delay parameters of the proposed single-bit full adder are 930.3-nW and 43.07-ps respectively.**

Keywords— Low power, delay, XNOR logic, full adder, RCA.

I. INTRODUCTION

As the technology and time advances the demand of low power and fast operating devices is increasing. Full adder is the basic combinational element of the electronics industry. For the fast operation of the signal processing integrated circuits (ICs), the basic algorithms such as convolution, multiplication, swapping etc. must be fast as much as possible. Full adder is the basic arithmetic circuit which is used in almost all algorithms. Based on logic styles being used, the designs of adder circuits are basically divided into two categories, (1) static and (2) dynamic style. The choice of using static or dynamic logic is dependent on many criteria than just its low-power performance, delay, testability, area and ease of design.

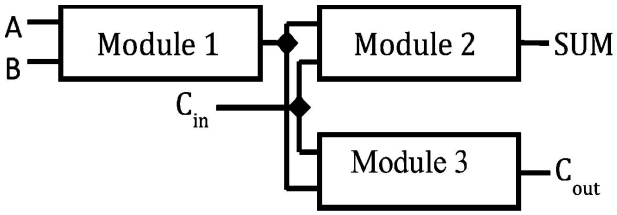
Static full adders show more reliability and simplicity with lesser energy requirement, but the on chip area requirement is usually more as compared to dynamic logic based adders [1], [2]. Whereas, dynamic full adders have some advantages over static full adders like fast switching speed, output having full swing voltage levels, no static power consumption etc. [1], [2].

There are many drawbacks related to static full adders i.e. performance, delay, power consumption in which delay and power are the main area of concern. So to improve the power and delay of the ICs, full adder should consume the minimum power and have the lowest delay. Thus, power and delay are the vital resources of an adder. Hence, optimizing these parameters has been the interesting topic for researchers and low power very-large scale integrated circuit (VLSI) designers over the years [9]-[10]. So designers try to save the power and lessen the delay.

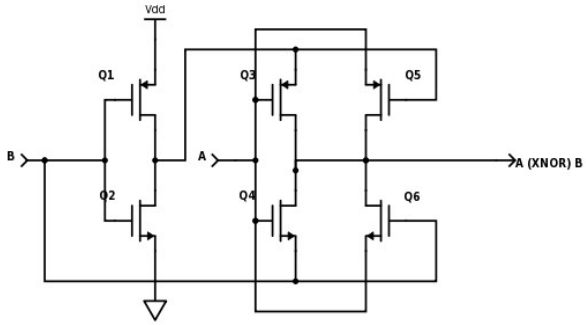
Power is one of the main resources of digital circuits hence design engineers try to save it. Switching activity, size of the transistor, intermediate node capacitances (diffusion, gate and wiring capacitances) are main resources of power dissipation in CMOS circuits [1]. At the device level power dissipation can be reduced by reducing the level of supply voltage and threshold voltage. However, lower supply voltage increases the delay problem and degrades the drivability of cascaded cells where as threshold voltage reduction increases the standby leakage currents. Transistor sizing is one of the best techniques to reduce power consumption [1], [2]. By selecting the optimum width to length (*W/L*) ratio of every individual transistor we can succeed in power saving [8].

In context to the single bit full adder design, various design techniques were investigated and compared with the new design [1]-[9]. Every design tends to favour one parameter at the cost of others. On the basis of output, full adder cells are mainly classified into two types. Transmission gate full adder(TGA), complimentary pass transistor logic (CPL), static complimentary metal-oxide-semiconductor (CMOS), dynamic CMOS, transmission function full adder (TFA), 14T and 16T full adders[5]-[7], [3], [16] lie under first type which have the full swing output voltage level. The second type (10T, 9T, 8T Full adders) is a group of full adders without full swing output [14], [16]-[19]. The group of first type full adders is having more number of transistors, high power consuming, large area as compared to second type.

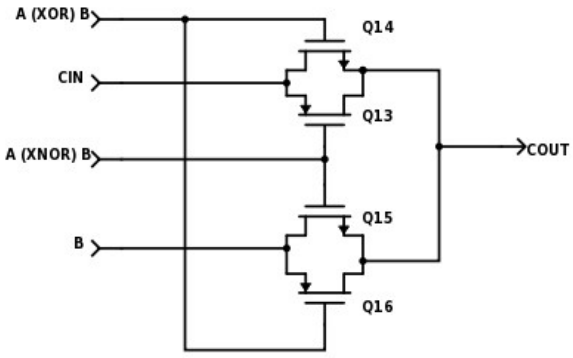
Complimentary CMOS, dynamic CMOS, CPL, TGA are the main conventional logic designs [1]-[2]. Complimentary CMOS (C-CMOS) is having the advantage of robustness against voltage scaling and arbitrary transistor sizing which is responsible for its reliable operation at low voltage while the disadvantages of C-CMOS are requirement of buffers, more number of transistor count (28T) and capacitances at input level [1]. Carry propagation delay of C-CMOS adder was reduced in Mirror adder design [2] with same power consumption and transistor count. CPL shows a better voltage



(a)



(b)



(c)

Figure.1 (a) Building blocks of proposed full adder, (b) Modified XNOR Module, (c) Carry Module

swing restoration by the use of 32 transistors but higher switching activity of intermediate nodes, overloading of inputs, high transistor count makes it inappropriate for low power applications [5], [7]. The main drawback of CPL is voltage degradation problem which was overcome in TGA with twenty transistors (20T) only [6], [8]. Other drawbacks of CPL are high power consumption and slow speed which remain a concern for designers. To overcome these problems later hybrid design styles were employed. Hybrid design contains more than one logic styles [11]-[14]. 14T full adder [3] and hybrid logic with static CMOS output drive full adder (HPSC) [4] are hybrid adders. Although these hybrid logic styles provide the full swing output but the poor driving capability makes them inappropriate for cascaded mode of operation. The main aim of the proposed design approach in this paper is to improve the energy and delay parameters as compared to

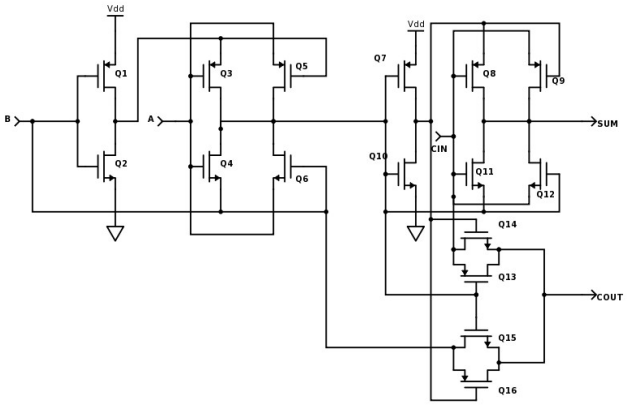


Figure. 2 Complete diagram of proposed full adder

existing designs. The circuit was implemented and simulated by Cadence Virtuoso simulator. Power consumption is reduced by deploying the weak inverters and delay is improved by the use of strong transmission gates. In *umc* 180nm technology power and delay for single bit full adder are calculated as 930.3-nW and 43.07-ns respectively for 1.8V supply. The design was also verified for 4-bit RCA.

II. PROPOSED FULL ADDER

Fig. 1(a) shows the basic structure of a full adder. Equation (1) describes the sum and carry outputs in the form of input variables. The proposed structure basically contains three modules. Modules 1-2 are XNOR logics which are responsible for the sum function and Module 3 is a carry module. Module 1 and Module 2 are generating the sum signal, by connecting in cascaded form and Module 3 is a Mux, designed by using the pass transistors.

$$SUM = A \oplus B \oplus Cin$$

$$\begin{aligned} Cout &= AB + BCin + CinA \\ &= Cin(A \oplus B) + AB \end{aligned} \quad (1)$$

A. Proposed XNOR Module

In the three module based proposed circuit, power consumption is mainly dominated by XNOR module. Therefore, XNOR module is designed such that, the power consumption is minimum. Fig. 1 (b) shows the modified XNOR circuit, where the power consumption is reduced by the use of weak inverters. A weak inverter is that which is having the small channel width, comprised of Q1 and Q2. Output of weak inverter is used to form a controlled inverter (using Q3, Q4). Q5 and Q6 form a level restorer which is responsible for the full swing of the output signal. XNOR/XOR topologies are discussed in [8] and [17]-[19]. XNOR topology in [17]-[19] uses 4T but its output is having the low logic swing problem.

The proposed modified XNOR module uses 6T in a different manner as compared to [8] and the proposed circuit consumes lesser power.

B. Proposed Carry Module

Carry signal is mainly responsible for the delay of the proposed full adder circuit. A carry generating module is

TABLE I
TRUTH TABLE OF 1-BIT FULL ADDER

A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE II
TRANSISTOR SIZES OF PROPOSED 1-BIT FULL ADDER

Tr. Name	Width(nm)	Length(nm)
Q1,Q3	800	180
Q2, Q4,	400	180
Q5, Q7	800	180
Q8, Q9,	400	180
Q6, Q10,	400	180
Q11, Q12	400	180
Q13, Q16	400	180
Q14, Q15	400	180

Shown in fig. 1 (c) which is composed of (Q13, Q14, Q15, Q16) pass transistors. In CMOS Design, pass transistors are known for the low power circuits [1]. The carry signal (C_{in}) passes only through a single transistor in every combination of input vector which reduces the carry propagation path. Reduction in the carry propagation path reduces the delay of carry signal.

III. OPERATION OF THE PROPOSED FULL ADDER

Fig. 2 shows a detailed circuit of the proposed full adder. Sum output is implemented by two cascaded XNOR modules. Signal B is applied to the weak inverter comprised of Q3, Q4. Input and output signals (B and B' respectively), of this weak inverter are used to construct the controlled inverter with Q3 and Q4 transistors. The output of the controlled inverter is XNOR of A and B but it is degraded one. To overcome this swing degradation problem pass transistors Q5 and Q6 are used. A p-MOS pass transistor (Q5) is used to get strong 1 at its output and n-MOS pass transistor (Q6) for strong 0 [1]. So the output of the XNOR module is having full swing levels. The output of the first XNOR module is applied as input to the second XNOR module for complete SUM function. Table I is the truth table for SUM and Cout functions in form of input variables. According to the truth Table-I the carry signal can be analyzed as following

If A=B, then C_{out}=B, else C_{out}=C_{in}.

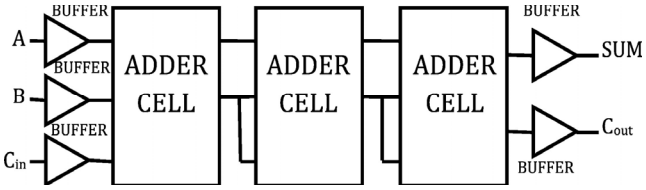


Fig.3 Three Stage Simulation test bench setup

The proposed single bit full adder may malfunction under low supply voltage when deployed to real time environment. This malfunctioning may occur because of the loading capacitance of cascaded adder cells or because of improper input to the driven cells. So to test the real time applications of the circuit a practical test bench set-up is shown in the fig. 3. To avoid the signal degradation in practical application conditions, three buffers are incorporated at the input stage and two at output stage [13], [20]. Output buffers ensure the proper loading effect while input buffers incorporate the input capacitances. The number of stages for test bench is set to three (detailed discussion in section IV-*B. Delay calculation*) because after third stage the delay of carry signal increased gradually. All possible input combinations were applied to the test bench at room temperature and worst case power and delay parameters are calculated.

IV. PERFORMANCE ANALYSIS OF PROPOSED ADDER

As *W/L* ratio of a transistor is varied, the power consumption also varies accordingly [1], [2]. Table II shows the *W/L* ratio of each individual transistor for the proposed circuit. Post layout simulations of modified hybrid full adder are done by Virtuoso simulator. In 180 nm technology minimum threshold voltage is 0.8V and break down voltage is 1.8V so simulation results were calculated by varying the supply voltage from 0.8V to 1.8V. Input–output waveforms of proposed full adder are shown in Fig. 4, Fig. 5 at 0.8V and 1.8V respectively, and dynamic power consumption is shown in the Fig. 8 for the same supply variation.

A. Power analysis

Total power consumption of a digital CMOS circuit is the sum of dynamic, static and short circuit power. Equation (2) is showing the total power consumption of a digital CMOS circuit. Although, dynamic power is the main source of power consumption in the proposed full adder circuit design.

$$P_{total}=P_{Dynamic}+P_{Static}+P_{Short\_Circuit}$$

$$P_{Dynamic}=V_{dd}F_{clock}\sum_{i}^{N}(\alpha_i)V_{iswing}C_{iLoad} \quad (2)$$

Where F_{Clock} is representing the clock frequency of the system, V_{iswing} is the voltage swing at intermediate nodes from *i* to *N* and C_{iLoad} is the load capacitance at node *i*. In CMOS circuits generally static power is due to leakage currents and biasing conditions, which is very low as compare to dynamic power in this proposed circuit. Dynamic power is the main component of power consumption here which arises due to switching activities of load capacitances. As the input vector

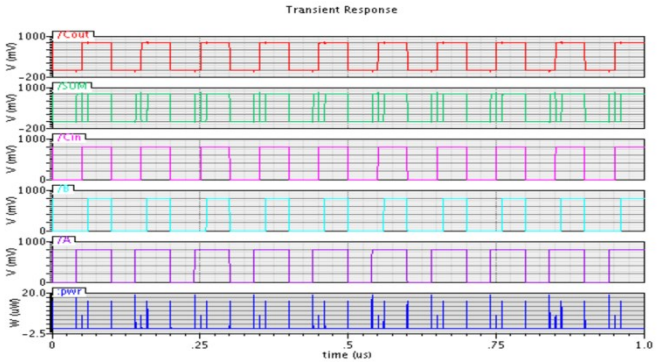


Fig.4 Input Output Waveform of proposed full adder at 0.8V supply

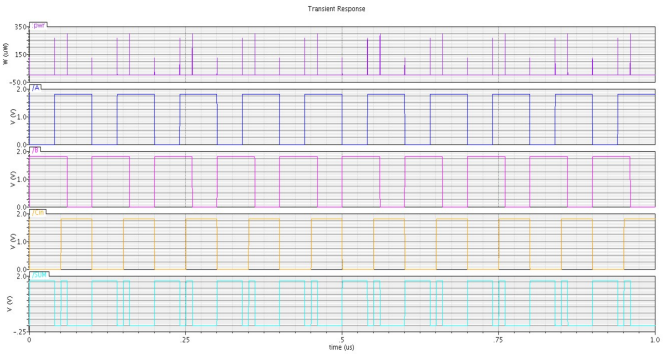


Fig. 5 Input Output wav form of proposed full adder at 1.8V supply

transits between high and low logics, the load capacitances show their charging and discharging behavior that is responsible for the dynamic power consumption. The dynamic power consumption can be reduced by optimizing the transistor size [8]. So in the proposed design weak inverters and strong pass transistors are deployed by setting a particular *W/L* ratio (according to table II) to reduce this dynamic power consumption.

B. Delay calculation

Propagation delay is the time taken by the carry module to generate the output signal. In the proposed circuit the carry signal delay is reduced by reducing the propagation path of the carry signal. The delay propagation path is reduced by deploying strong transmission gates.

An R-C equivalent circuit of a carry propagation module is shown in the fig. 7 (a). R is a linear resistance and C_1, C_2 are parasitic capacitances at input, output nodes. By taking the voltage source V_{in} as a step waveform and C_L as loading capacitance, the total delay (given by *tpd(m)*) of *m*-cascaded stages can be represented by Elmore's Delay model [3] as follows

$$t_{pd}(m) = 0.69\left[R(C_1 + C_2)\frac{m(m+1)}{2} + mR(C_L - C_1)\right] \quad (3)$$

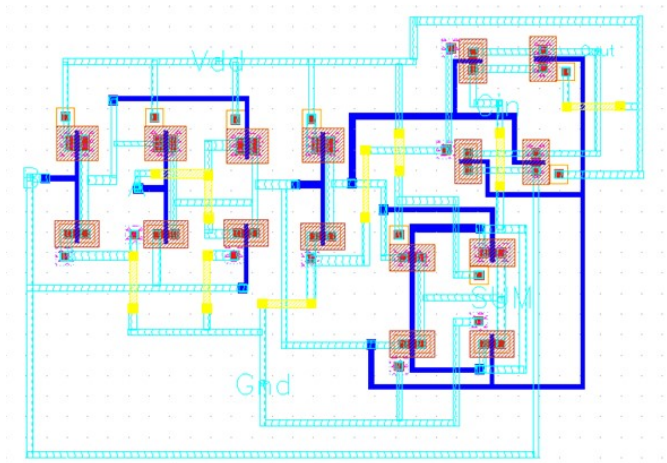


Fig. 6 Layout of Proposed Full Adder

From the above equation it is clear that the delay of the proposed circuit is proportional to square of *m* when the numbers of stages are increased in cascaded form. Post layout Simulation results were done without any load capacitance. The worst case delay is 43.07-ns of the proposed adder.

By incorporating the intermediate buffers at proper stages we can reduce the delay significantly. After inserting the buffers at proper stages the Elmore equation modifies according to equation (4) as follows

$$t_{pd}(m)total = t_{pd}(m) + t_{pdbuf}$$

$$= 0.69\left[R(C_1 + C_2)\frac{m(m+1)}{2} + mR\left(C_{inbuf} - C_1\right)\right] + t_{pdbuf} \quad (4)$$

Where t_{pdbuf} is the delay of buffers, which is constant. To get the optimum number of cascaded stages, differentiating the average delay equation (4) with respect to *m* gives a resultant of approximately 3 because of which we took 3-stage test bench for simulation purpose.

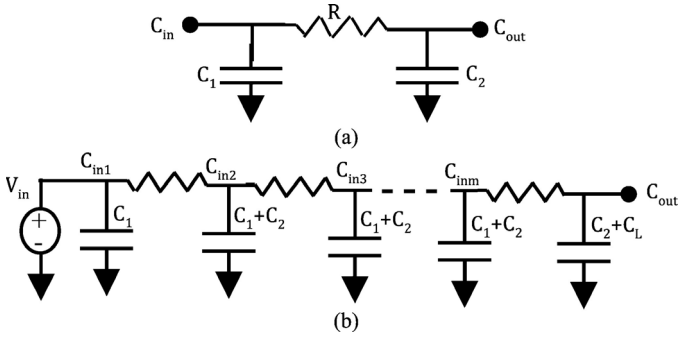


Fig.7 (a) R-C Equivalent of Transmission gate which causes delay, (b) R-C Equivalent of *m*-stage cascaded.

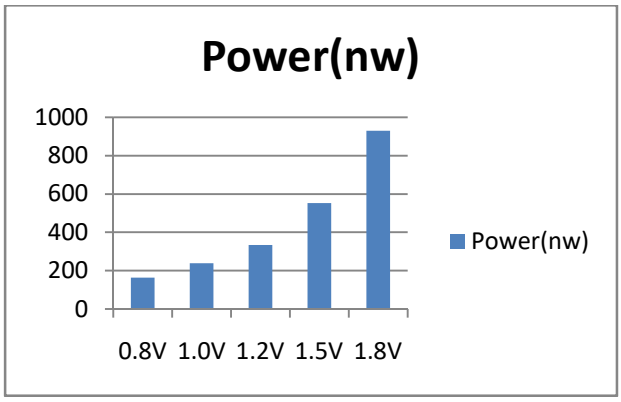


Fig. 8 Dynamic power variation of proposed full adder while varying the supply from 0.8V to 1.8V.

Table III shows all the calculated parameters of the proposed 1-Bit full adder in *umc* 180-nm technology.

Table III
Parameters of proposed 1-Bit Full adder

	Tr. count	Power (nW)	Delay (nS)	PDP (fJ)	Area (μm^2)
Proposed Adder	16	930.3	43.07	40.06	116.23

V. 4-BIT RIPPLE CARRY ADDER

A schematic and layout diagram of 4 bit ripple carry adder is shown in the fig. 9. In an RCA the output carry is forwarded to the next stage as an input carry. The 4 bit RCA was designed using four single bit proposed adders in *umc* 180nm environment. Post layout simulation is done at 1.8V supply and for all different input combinations. Worst case delay and power parameters are measured as 48.91-ns and 3.90-µW respectively.

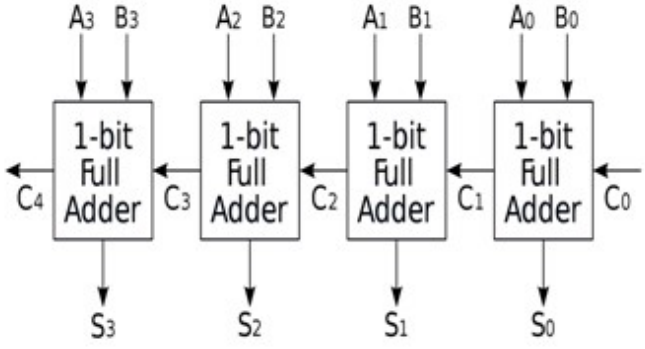


Fig. 9 Building block diagram of 4-Bit Ripple Carry Adder

VI. CONCLUSION

In this paper an ultra low power high speed full adder is emphasized using modified XNOR modules. The design is also verified for 4-Bit ripple carry adder. Post layout simulations were done using Cadence Virtuoso tools in 180-nm technology. Simulation results show that the new design offers improved PDP as compared to existing logics. Strong transmission gates driven by weak inverters show a high switching speed of 43.07-ns at 1.8V supply. The proposed circuitry was used to implement a 4-bit RCA.

ACKNOWLEDGEMENT

The author would like to thank the Electronics & Communication Engineering Department of Maulana Azad National Institute of Technology, Bhopal for providing simulation facility.

REFERENCES

[1] N. H. E. Weste, D. Harris, and A. Banerjee, *CMOS VLSI Design:A Circuits and Systems Perspective*, 3rd ed. Delhi, India: Pearson Education, 2006.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Delhi, India: Pearson Education,2003.

[3] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in *Proc. IEEE Workshop Signal Process. Syst. (SiPS)*,Taipei, Taiwan, Oct. 1999, pp. 713–722.

[4] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. Int. Symp. Circuits Syst.*, May 2003, pp. 317–320.

[5] R. Zimmermann and W. Fichtner, "Low power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[6] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEE Proc.-Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[8] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[9] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Intgr. (VLSI) Syst*.,vol. 14, no. 12, pp. 1309-1321, Dec. 2006.

[10] S. Wairya, R. K. Nagaria, and S. Tiwari, "New design methodologies for high-speed low voltage 1 bit CMOS Full Adder circuits," *International Journal of Computer Technology and Application*, vol. 2, no. 3, pp. 190–198, 2011.

[11] M. Aguirre-Hernandez and M. Linares Aranda, "CMOS full-adders for energy-efficient arithmetic applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 718–721, Apr. 2011.

[12] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in *Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst.*, vol. 13. Apr. 2007, pp. 1–4.

[13] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *VLSI J. Integr.*, vol. 42, no. 4, pp. 457–467, Sep. 2009.

[14] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," *IEEE Trans.*

Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.

[15] S. R. Chowdhury, A. Banerjee, A. Roy, and H. Saha, "A high speed 8 transistor Full Adder design using novel 3 transistor XOR gates," *International Journal of Electronics, Circuits and Systems, WASET Fall*, pp. 217–223, 2008.

[16] Subodh Wairya, Rajendra Kumar Nagaria, and Sudarshan Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Low Voltage VLSI Design," VLSI Design,vol. 2012, Article ID 173079, 18 pages, 2012.

[17] S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder circuit," in *Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUiCONE)*, Dec. 2011, pp. 1–7.

[18] S. Goel, M. Elgamel, and M. A. Bayoumi, "Novel design methodology for high-performance XOR-XNOR circuit design," in *Proc. 16th Symp. Integr. Circuits Syst. Design (SBCCI)*, Sep. 2003, pp. 71–76.

[19] J.-M. Wang, S.-C. Fang, and W.-S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 780–786, Jul. 1994.

[20] K. Navi *et al.*, "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter," *Microelectron. J.*, vol. 40, no. 10, pp. 1441–1448, Oct. 2009..