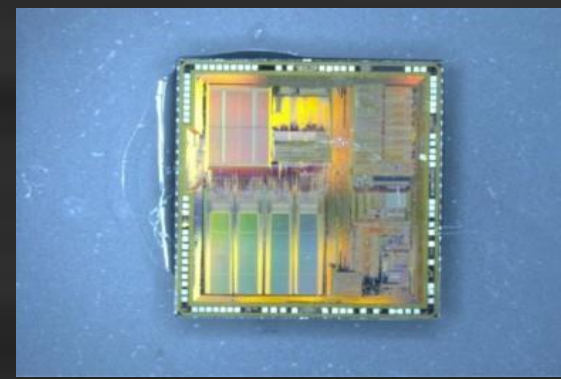
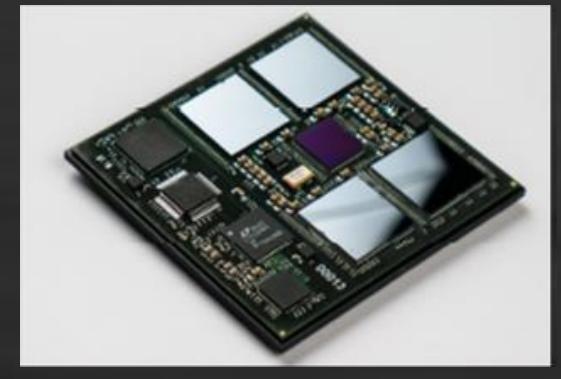


Heterogeneous MCM



Die Extraction and Reassembly



Semiconductor Packaging

i3 Microsystems Inc.

Heterogeneous System-In-Package (HSIP) Technology

Charles Woychik, Robert Mundella, Keith Kunard, Victor Vilar, Justin Borski and Robert Nead

i3 Microsystems, Inc.

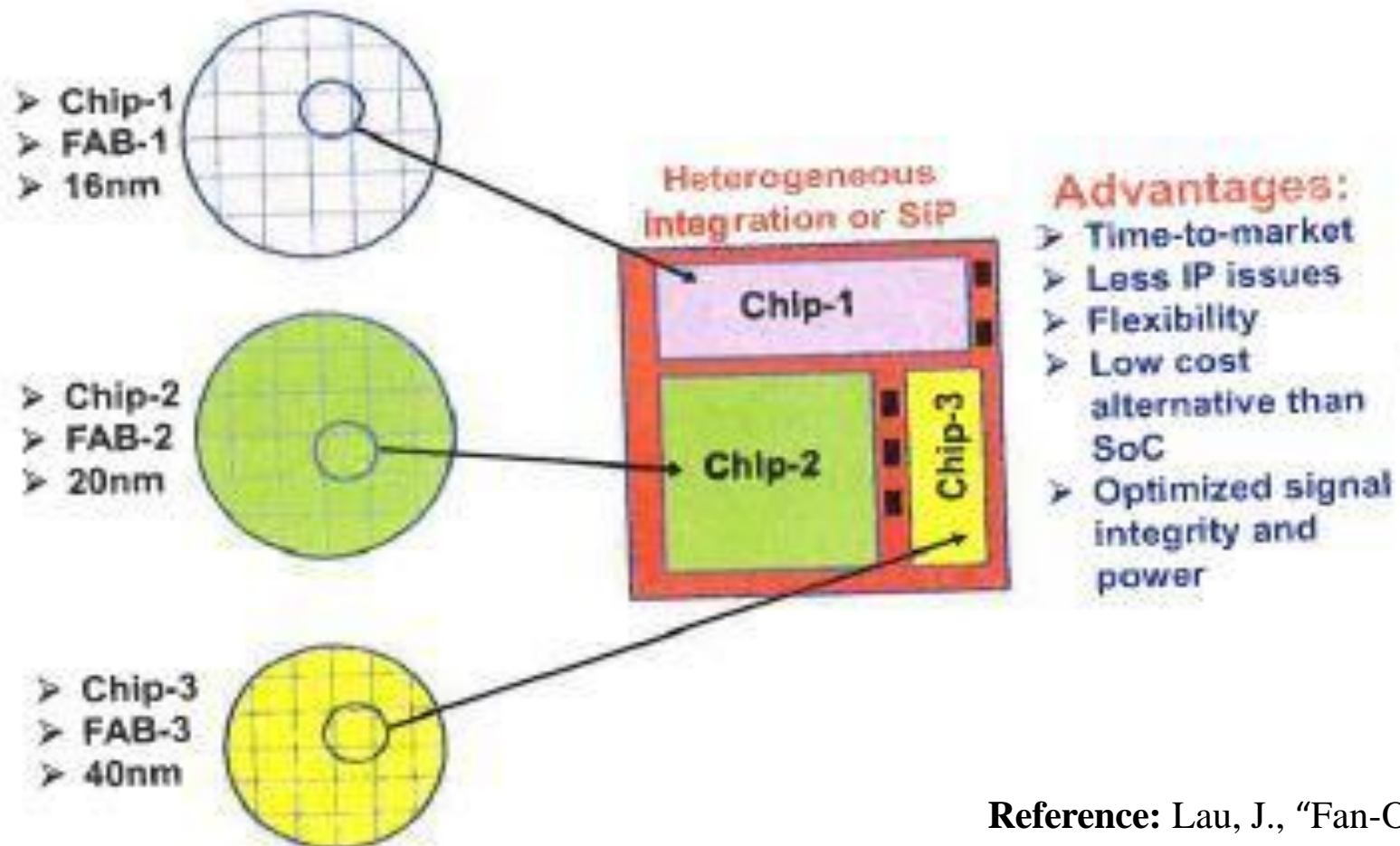
9900 16th Street North

St. Petersburg, FL 33716

Outline

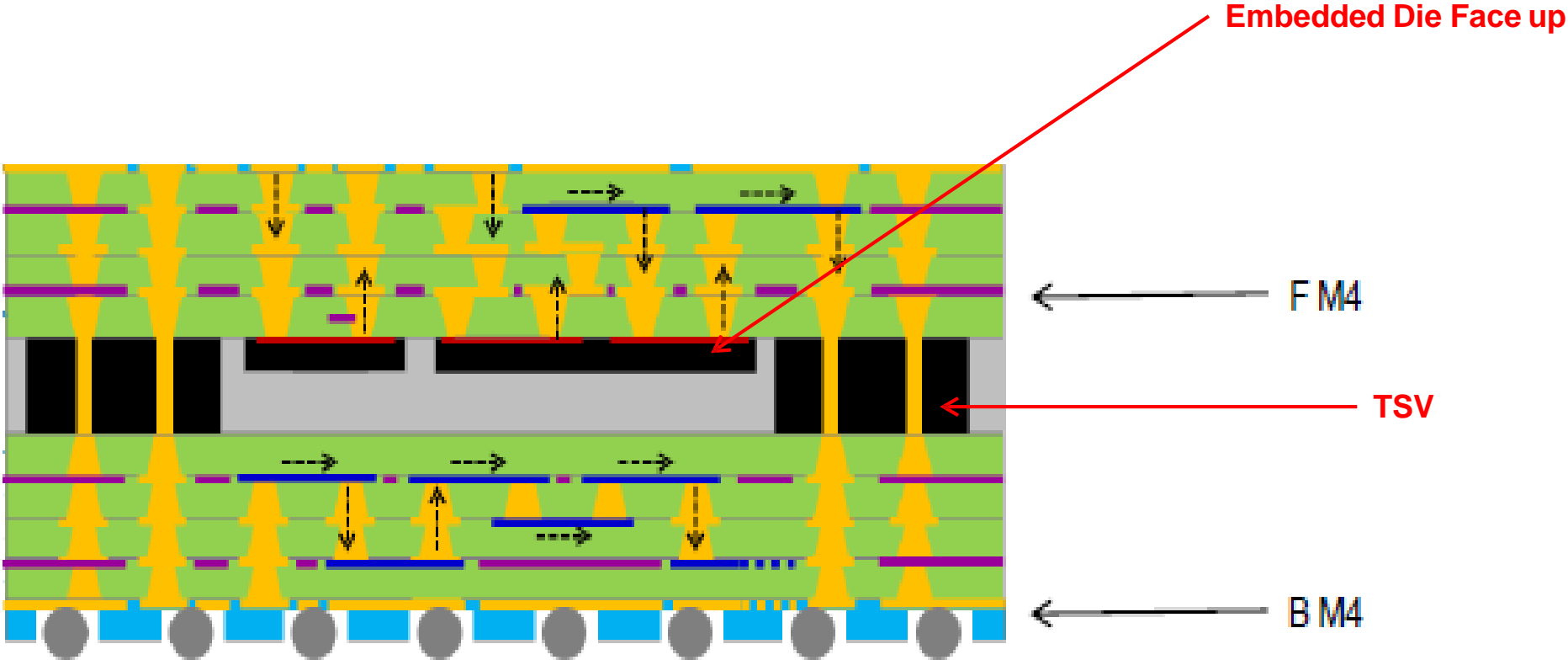
- Introduction
- Test Vehicle Design
- HSIP Module Build
- Results
- Conclusions
- Acknowledgements

HSIP Integration Approach



Reference: Lau, J., "Fan-Out Wafer-Level Packaging," Springer Nature Singapore Pte Ltd., 2018. Chapter 11, pp. 269-303.

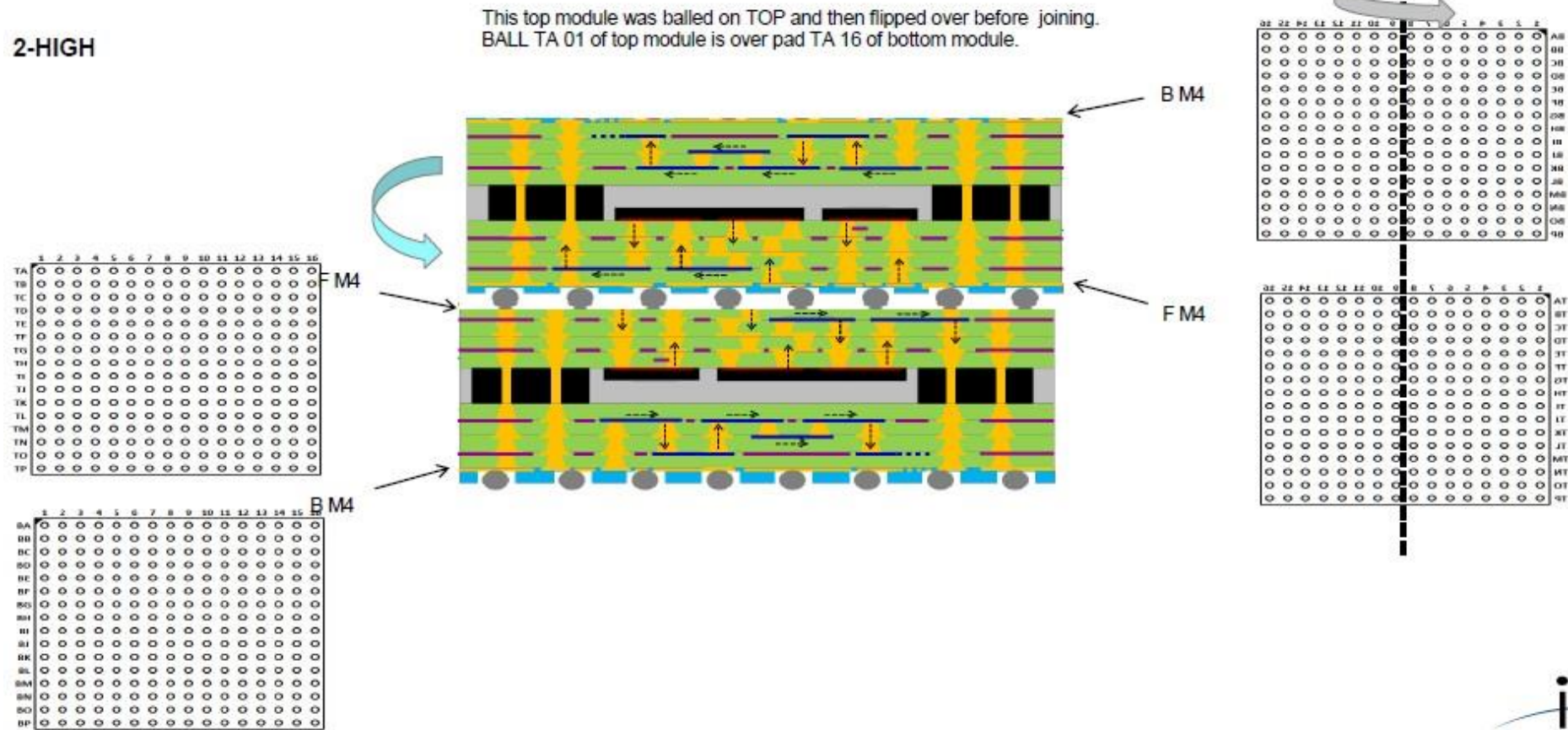
Test Vehicle Design - Single Slice



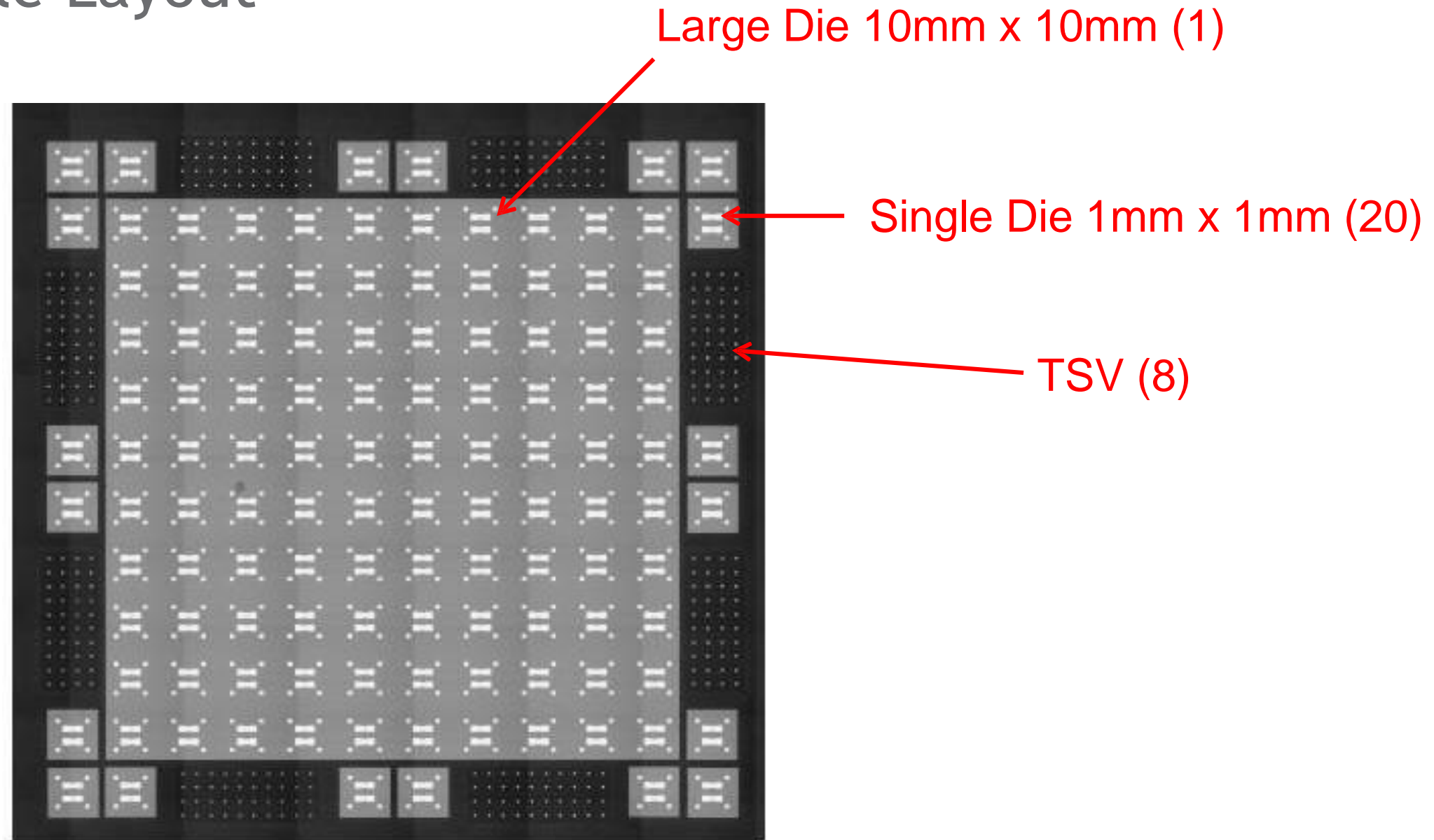
Test Vehicle Design - Double Slice

Need Fiducials and POD Notes to cover 1 high AND 2-HIGH configurations

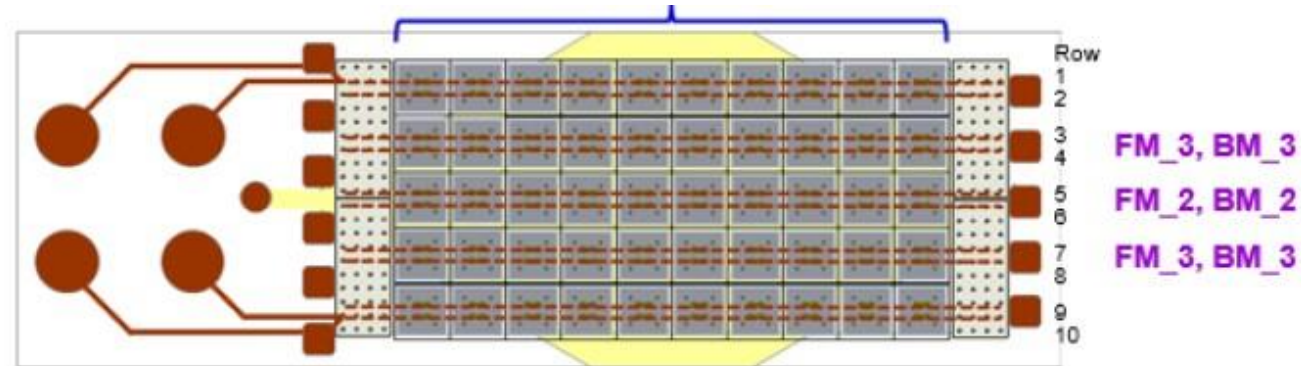
2-HIGH



RTV Molded Module Layout

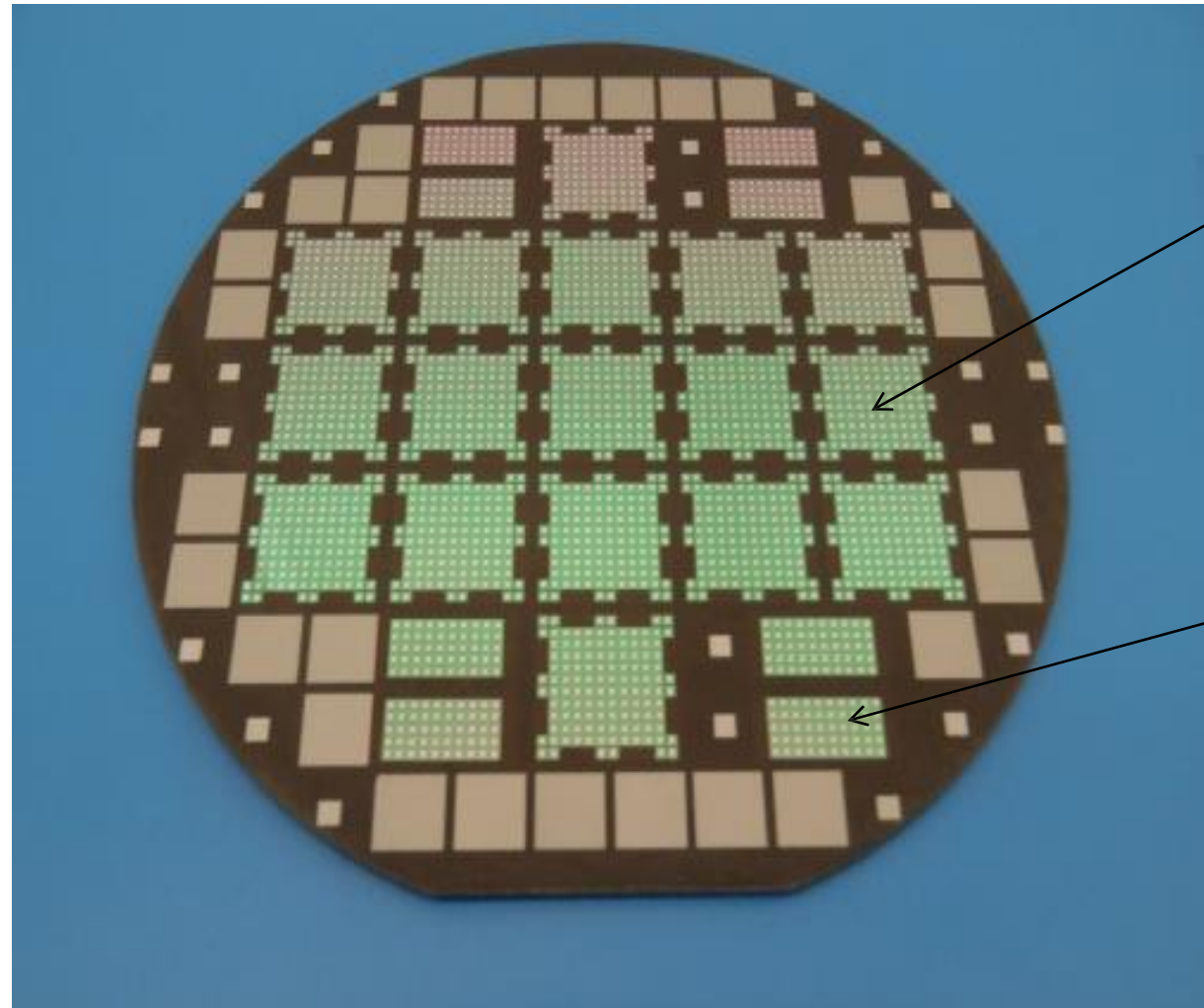


CITC Module Layout



Rows	TOP/Front	BOT/Back
1, 2, 9, and 10	Chip Side Via stitch 4 high vias like TV Net PP4-4-4	Non chip side via stitch 3 high vias like TV Net PP15-6-3
3, 4, 7, and 8 FM_3 BM_3	Chip Side Via stitch 3 high vias like TV Net PP3-4-3	Non chip side via stitch 2 high vias like TV Net PP14-6-2
5 and 6 FM_2 BM_2	Chip Side Via stitch 2 high vias like TV Net PP2-4-2	Non chip side via stitch 1 high vias like TV Net PP13-6-1

Embedded Core Layout



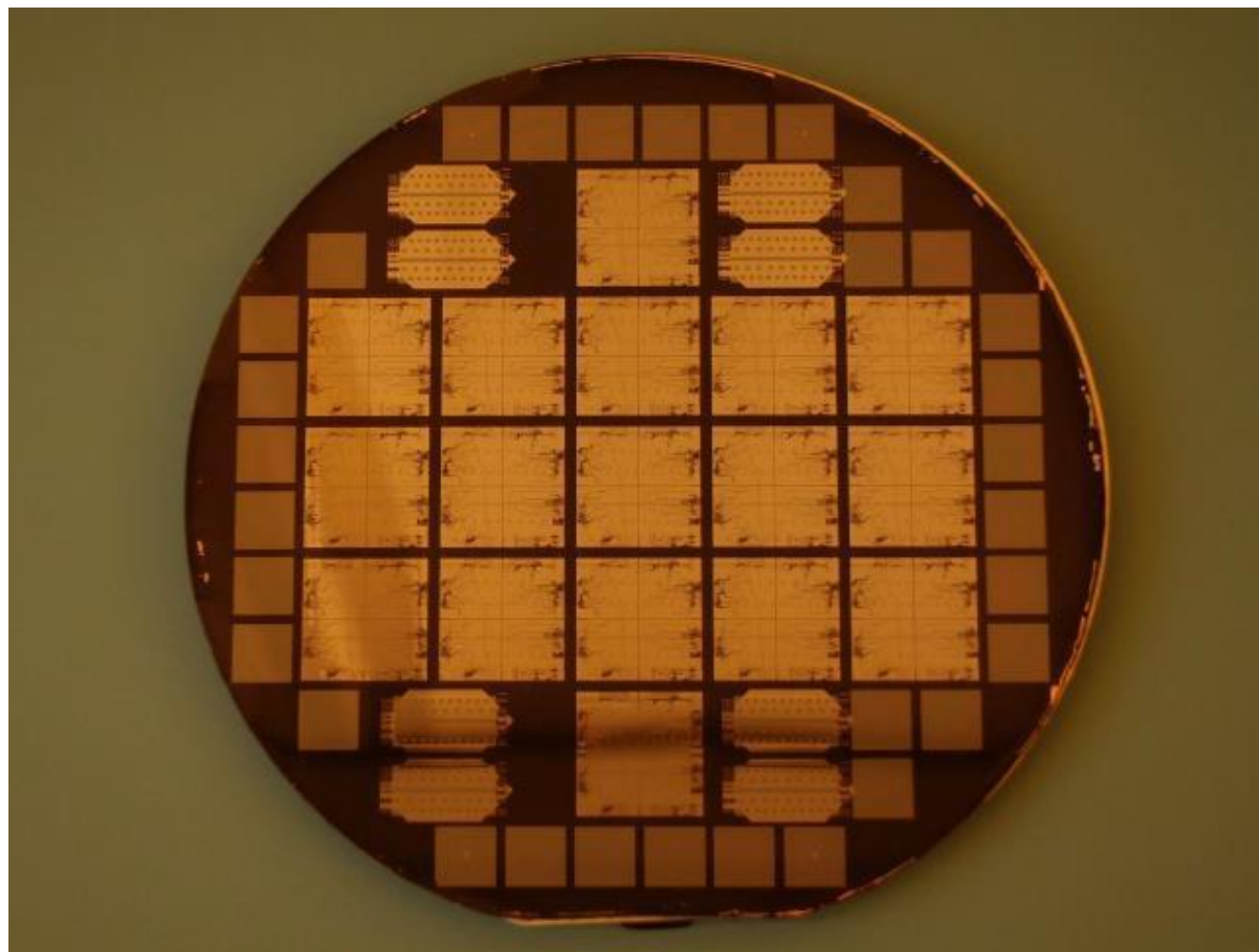
RTV – 17 module sites

CITC – 8 module sites

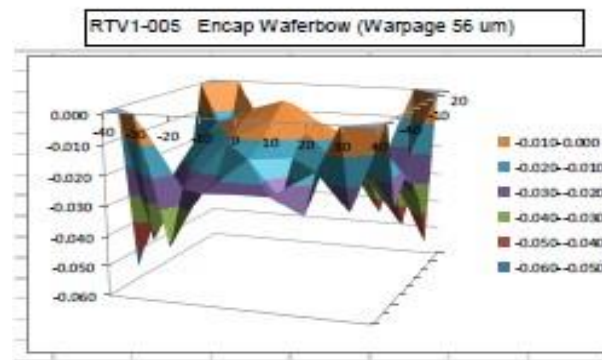
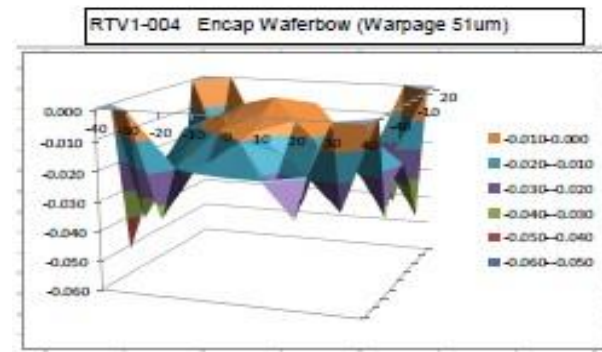
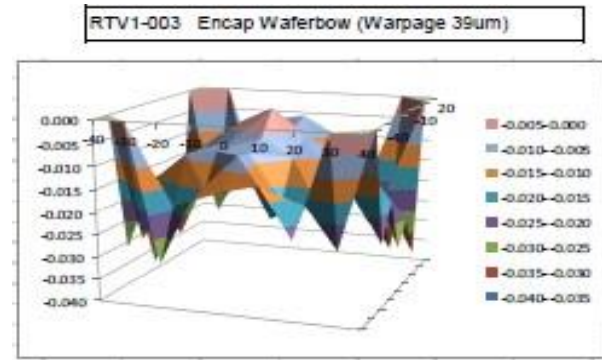
Processing Conditions

- ❑ RTV-03 low cure temperatures and long bake times
- ❑ RTV-04 higher cure temperatures and shorter bake times
- ❑ RTV-05 higher cure temperatures and shorter bake times on a new equipment set

Wafer with Backside Buildup Layer (BL1)

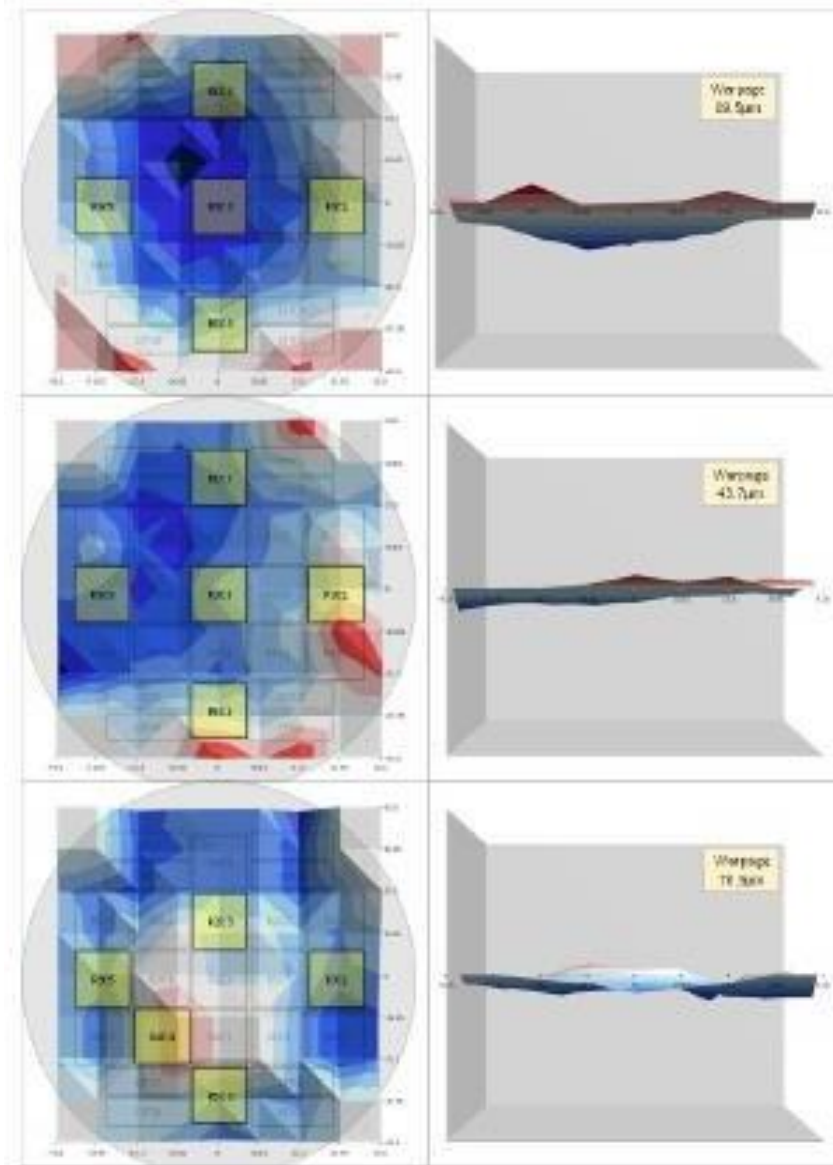


Warpage of the Reconstituted Wafer



- Warpage for RTV-03 is 38.5um
- Warpage for RTV-04 is 51.4um
- Warpage for RTV-05 is 56.9um

Warpage after Completion of Entire Buildup Layers



- Warpage for RTV-03 is 89.5um
- Warpage for RTV-04 is 43.7um
- Warpage for RTV-05 is 70.9um

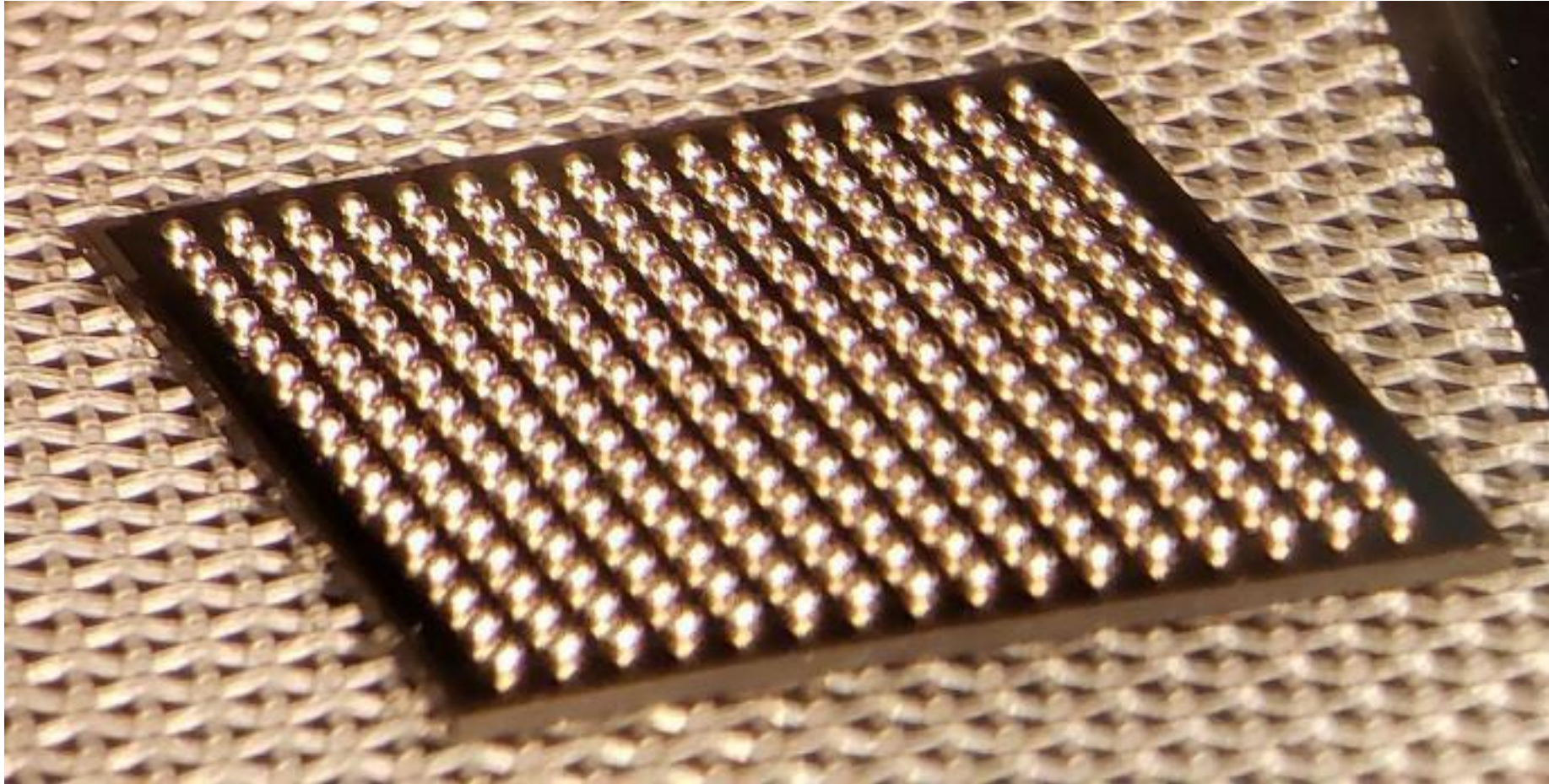
Warpage Measurement of Individual Modules

RTV1-003	
Final Module Bow	
R1C3	-0.4
R3C5	-2.2
R3C3	-3.8
R3C1	-1.7
R5C3	1.1
Avg	-1.40
Min	-3.8
Max	1.1

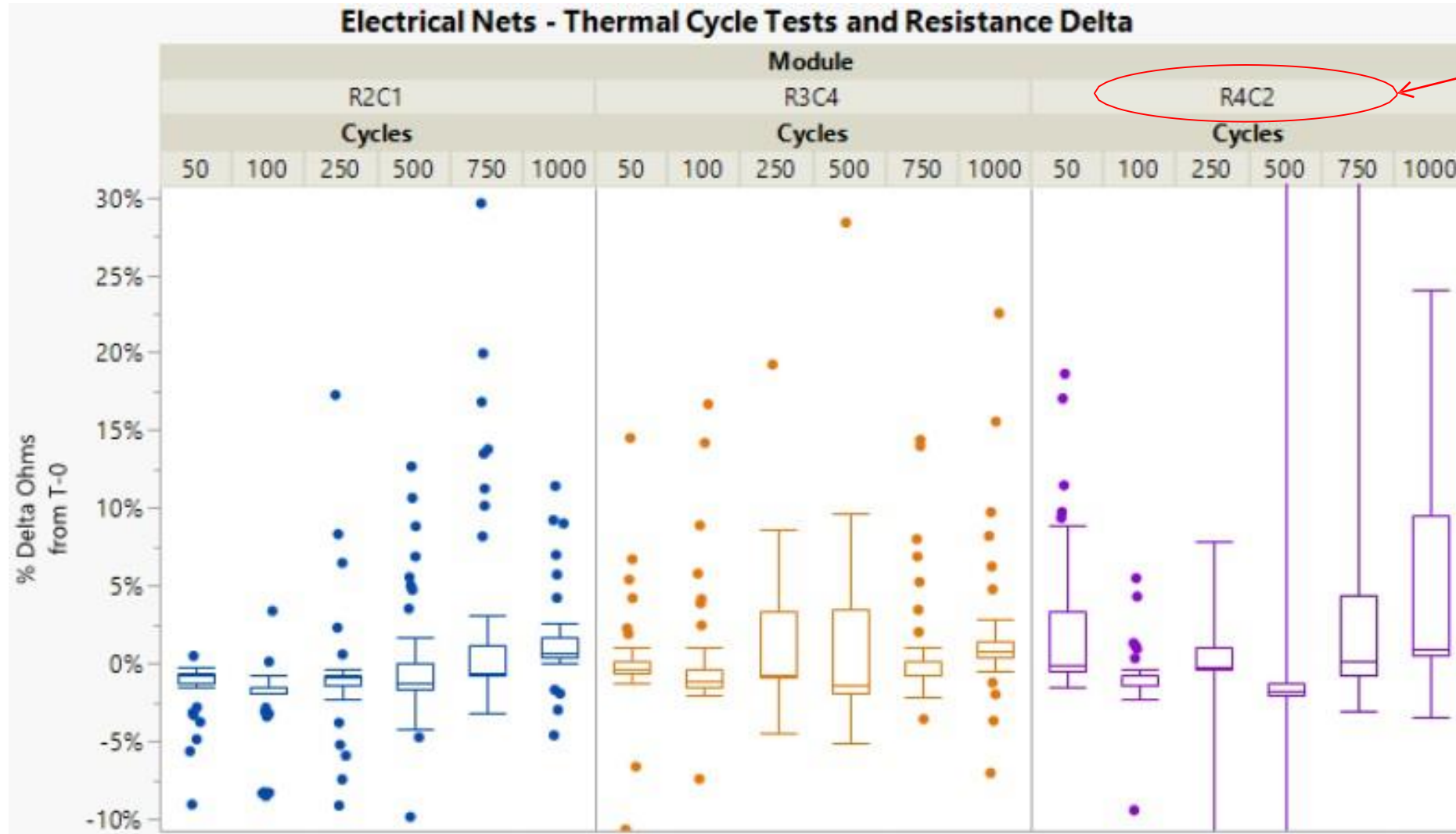
RTV1-004	
Final Module Bow	
R1C3	7.3
R3C5	-8.9
R3C3	-8.8
R3C1	3.4
R5C3	7.5
Avg	0.10
Min	-8.9
Max	7.5

RTV1-005	
Final Module Bow	
R2C3	7.0
R3C5	2.8
R4C4	3.1
R3C1	2.9
R5C3	11.4
Avg	5.44
Min	2.8
Max	11.4

BGA Attach

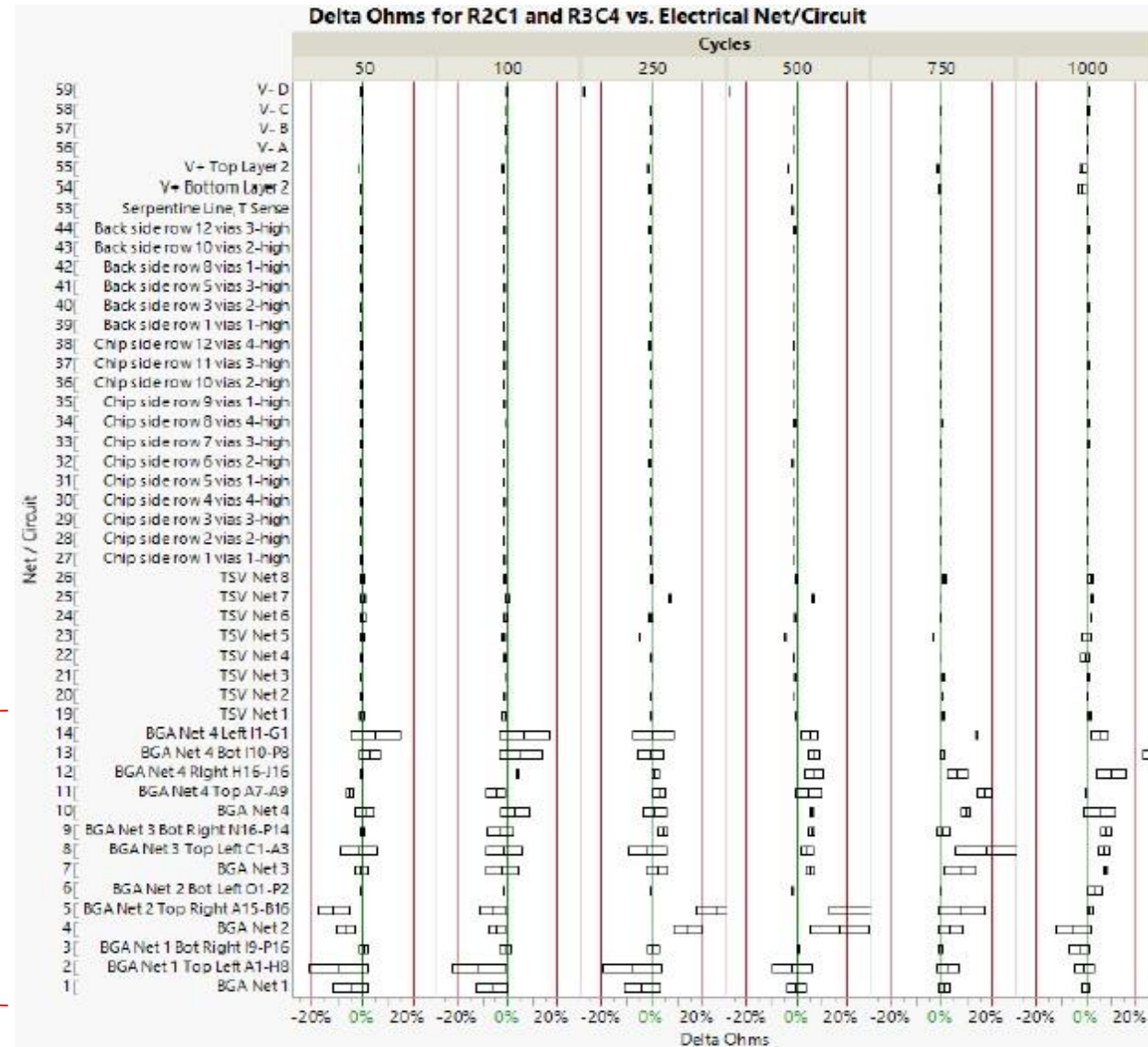


DTC Test results to 1000 cycles



Excessive Rework

DTC Testing of Modules R2C1 and R3C4 (No BGA rework)



Conclusions

- ❑ HSIP technology offers tremendous flexibility to accommodate different die types, sizes to produce a high performance high density multi-chip package using FOWLP.
- ❑ Process capable to produce a flat HSIP with good electrical circuit when using RTV-03 conditions (low bake, longer times).
- ❑ Early DTC sniff testing shows that modules subjected to a qualified BGA attach process are showing good reliability up to 1000 cycles. Testing will continue to 1000 cycles and beyond.
- ❑ Future work will concentrate on stacking modules and further testing under standard JEDEC conditions (T/C 0 to 100C, -40 to 125C).

Acknowledgements

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- Larry Black, Program Mgr.
- Chuck Baab, Process Engr.

Thank You!

Charles Woychik, Ph.D.

i3 Microsystems, Inc.

St. Petersburg, FL 33716

Charles.Woychik@i3microsystems.com